9.12 First we estimate the computational workload. The total workload is

$$N_{op} = 352.8 + 352.8 + 352.8 + 705.6 = 1.764 \text{ MOp/s}$$

The clock rate in cut A-A' is $f_{CL} = N_{op}\, W_d = 1.764 \cdot 20 \approx 35.3$ MHz

The bit rate in A-A' is $(2 + 2)\, f_{CL} = 4 \cdot 35.3 = 141.2$ Mbit/s

The bit rate in B-B' is $f_{mem}\, W_{mem}$

Stage	1	2	3	4
Order	17	9	5	5
no. adaptors	8	4	2	2
frequency	44.1	88.2	176.4	352.8
kOPS	352.8	352.8	352.8	705.6

If we choose $W_{mem} = 20$ bit we will have $f_{mem} = \frac{141.2}{20} \approx 7.1$ MHz

To get $f_{mem} < 20$ MHz we must select $W_{mem} > \frac{141.2}{20} \approx 7.1$ bit