12.1 The number of dice per wafer is

$$N_{Dice} \approx \pi(\frac{D_w}{2L_c} - 1)^2 = \pi(\frac{8 \cdot 25.4}{2\,L_c} - 1)^2 = 561,\ 263,\ \text{and}\ 167\ \text{dice.}$$

The active area d is close to 1 for a high-density chip. Thus, $d\ A\ D \approx 0.95\ \text{A}\ 0.03 > 1$. Hence, we use Murphy-Moores model for the yield

$$Y = 0.5\left[\frac{1 - e^{-dAD}}{dAD}\right]^2 + 0.5\ \text{e}^{-\sqrt{dAD}}$$

We have: $d\ A\ D = 1.425$, 2.85, and 4.275. The yield is estimated to: 29.4%, 14.7%, and 9.0%. The cost is estimated to: \$600 Y/N_{dice} = \$4.66, \$15.52, and \$39.92 per die. Further, costs for testing, bounding, and packaging are incurred. For a small die, the cost of the package may be dominant.

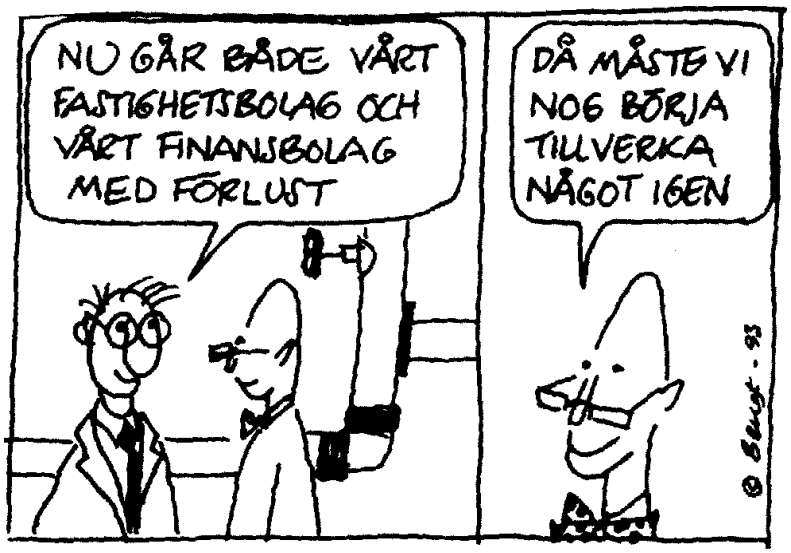
12.4 The excess junction temperature (above 25 °C) is: $T_j = 172 \cdot 0.4 = 69$ °C. The contribution from excess temperature, process spread, and reduced voltage is

$$\tau_{CL\ req} = (1+3.75\ 10^{-3} \cdot 69)(1+0.35)(1+0.3 \cdot 0.25)\ \tau_{CL\ design} =$$

$$= 1.2588 \cdot 1.35 \cdot 1.075\ \tau_{CL\ design} = 1.827\ \tau_{CL\ design}$$

$$f_{CL\ design} = 1.827 \cdot f_{CL\ req} = 1.827 \cdot 50 = 91.4\ \text{MHz}$$

Thus, the circuit should be designed with nominal parameter values to run with a clock frequency that exceeds the required frequency with 83%.



"Now when our real estate and finance branches are in the red we may have to start to manufacturing something"