1.10

```
entity Full_Adder is
    port(X, Y, Carry_in: in bit; Sum, Carry: out bit);
end  Full_Adder;

architecture Behavioral_View of Full_Adder is
begin
    process
          variable n: integer;
          constant Sum_vector: bit_vector (0 to 3) := "0101";
          constant Carry_vector: bit_vector (0 to 3) := "0011";
begin
          wait on X, Y, Carry_in;
          n :=0;
          if X = '1' then n := n + 1; end if;
          if Y = '1' then n := n + 1; end if;
          if Carry_in = '1' then n := n + 1; end if;
          Sum <= Sum_vector(n) after 3 ns;
          Carry <= Carry_vector(n) after 2 ns;
    end process;
end Behavioral_View;

architecture Data_Flow_View of Full_Adder is
signal Temp: bit;
begin
    Temp <= X or Y after 1 ns;
    Sum <= Temp or Carry_in after 2 ns;
Carry <= (X or Y) or (Temp and Carry_in) after 1 ns;
    end process;
end Data_Flow_View;

architecture Structural_View of Full_Adder is
component Half_Adder port(A, B: in bit; S, C: out bit);
end component;
component OR_Gate port(A, B: in bit; Out: out bit);
end component;
signal Temp1, Temp2, Temp3: bit;
begin
U1:     Half_Adder port map(X, Y, Temp1, Temp2);
U2:     Half_Adder port map(Temp3, Carry_in, Temp3, Sum);
U3:     OR_Gate port map(Temp1, Temp3, Carry);
end Structural_View;
```