

9.18 To verify the FFT architecture alternatives, we use an 8-point FFT.

Architecture 1:

- A butterfly PE shall always use data from two different RAMs.
- Butterflies from 0 to $N/4 - 1$ are assigned to PE0 and rest to PE1.

The memory assignment can be done with the exclusion graph method (See Chapter 7.11).

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|-------------|---|-------|-------|-------|-------|-------|-------|-------|
| Data index | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| Data $x(i)$ | ● | ● | ● | ● | ● | ● | ● | ● |
| RAM 0 | | RAM 1 | RAM 1 | RAM 0 | RAM 1 | RAM 0 | RAM 0 | RAM 1 |

Memory assignment

The assignment for the PEs are done by the requirement 2.

We can verify that all data come from different RAMs, for example, at the first stage, data pairs $\{x(0), x(4)\}$, $\{x(1), x(5)\}$, $\{x(2), x(6)\}$, and $\{x(3), x(7)\}$ come from both RAMs. The verification for the second and the last stage are left to the readers.

Architecture 2:

- The variables with indices 0 to $N/2 - 1$ are assigned to RAM0 and the rest to RAM1.
- Butterflies 0 to $N/4 - 1$ are assigned to PE0 and the rest to PE1.

At the first stage, data pairs $\{x(0), x(4)\}$, $\{x(1), x(5)\}$, $\{x(2), x(6)\}$, and $\{x(3), x(7)\}$ come from both RAMs. At the second stage, data pairs $\{x(0), x(2)\}$ and $\{x(1), x(3)\}$ come from RAM0 and the rest from RAM1. At the last stage, data pairs $\{x(0), x(1)\}$ and $\{x(2), x(3)\}$ come from RAM0 and the rest from RAM1, i.e., after the first stage, we have two separated 4-point FFTs on two different PEs.

Architecture 3:

- A butterfly PE shall always use data from two different RAMs.
- A RAM is not connected to both inputs of a butterfly PE.

This architecture has less restriction than that of Architecture 1, where PEs are assigned to butterflies.

Architecture 4:

- The variables with indices 0 to $N/2 - 1$ are assigned to RAM0 and the rest to RAM1.
- A RAM is not connected to both inputs of a butterfly PE.

It is impossible to implement FFT with this architecture. For example, at the last stage, the data pairs $\{x(0), x(1)\}$ should be processed in a butterfly PE. According to the first restriction, $\{x(0), x(1)\}$ should be stored in RAM0, which is not allowed according to the second restriction.