9.13 a) The number of 1-D DCT that have to be computed per second is

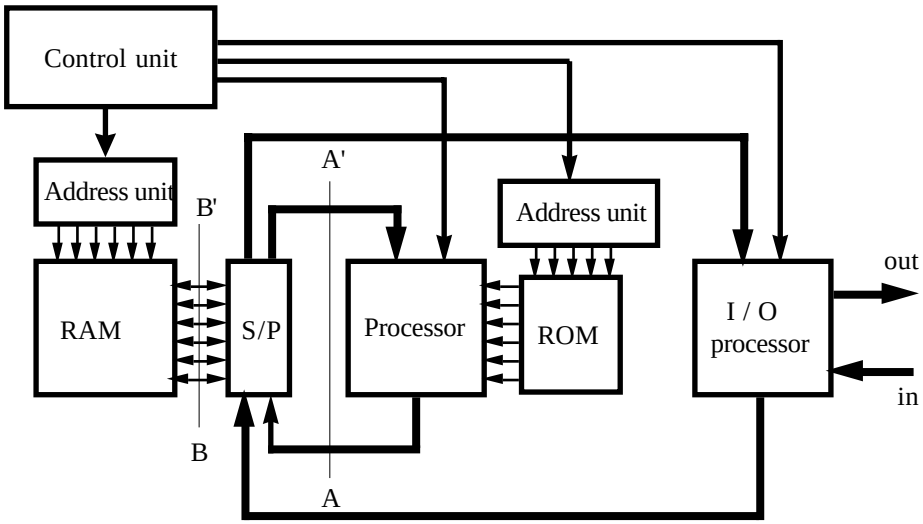
$$N_{tot} = (16 + 16 + 2) \cdot 240000$$

That is: 16 + 16 1-D DCT. We looses two cycles between the row and column computations because of the pipelining of the processors. The execution time for one processor is $\frac{14}{120\,10^6}$ at maximal clock frequency, i.e., we can compute $\frac{120\,10^6}{14} = 8.57\ 10^6$ 1-D DCT/s. The required number of processors is

$$N_p = \frac{34 \cdot 240000 \cdot 14}{120\,10^6} \approx 0.952 < 1$$

Thus, one processor is enough. The processor schedule becomes sequential, i.e., any feasible schedule is acceptable.

b)



c) The number of bits per second passing to and back from the processor is: 34 · 240000 · 14 = 114.24 Mbit/s. The processor must operate at 114 MHz.

d) Through the cut A-A': (16 + 16) 34·240000·14 = 3.66 Gbit/s.
Through B-B'

$$\frac{N_m \cdot W_m}{T_{RAM}} = \frac{N_m \cdot W_m}{17\ 10^{-9}} \Rightarrow N_m = \frac{3.66\ 10^9 \cdot 17\ 10^{-9}}{W_m}$$

We select $W_m = 12 \Rightarrow N_m \approx 5.18$

e) The memory must hold a whole 16 × 16 data matrix, i.e.,
16 · 16 · 12 = 3072 bits.

f) We select 8 RAMs each with 32 $\times$ 12-bit words. This selection yields a simple organization of the memories.

g) We have already selected W_m = 12. The required access frequency for the memories is $3.65568\ 10^9 = 8 \cdot 12 \cdot f_m$

$\Rightarrow f_m$ = 38 MHz