

2 VLSI CIRCUIT TECHNOLOGIES

2.1 From Eq.(2.5) and (2.6) we have: $\tau \approx \frac{4 C_L}{\beta} \frac{V_{DD}}{(V_{DD} - |V_T|)^2}$

$$\frac{f_2}{f_1} = \frac{\tau_1}{\tau_2} = \frac{\frac{V_{DD1}}{(V_{DD1} - |V_T|)^2}}{\frac{V_{DD2}}{(V_{DD2} - |V_T|)^2}} \approx \frac{\frac{5}{(5 - 0.75)^2}}{\frac{3.3}{(3.3 - 0.75)^2}} \approx 0.545 \Rightarrow$$

$$\Rightarrow f_2 \approx 0.545 \cdot 100 = 54.5 \text{ MHz}$$

For the sake of simplicity, we assume that the capacitors involved do not change with the supply voltage. Note that, in practice, this assumption is not entirely true.

$$\frac{P_1}{P_2} = \frac{f_1 C_1 V_{DD1}^2}{f_2 C_2 V_{DD2}^2} \approx \frac{5^2}{0.545 \cdot 3.3^2} \approx 4.21 \Rightarrow P_2 \approx \frac{1.3}{4.21} \approx 285 \text{ mW}$$

2.3 a) $P_{tot} = N \cdot f \cdot P_{gate} \Rightarrow N = \frac{P_{tot}}{P_{gate} \cdot f} = N = \frac{2}{6.5 \cdot 10^{-6} \cdot 80} = 3.8462 \cdot 10^3$

b) $\frac{P_1}{P_2} = \frac{f_1 C_1 V_{DD1}^2}{f_1 C_1 V_{DD2}^2} = \frac{V_{DD1}^2}{V_{DD2}^2}$

$$N = \frac{P_{tot} \cdot \frac{V_{DD1}^2}{V_{DD2}^2}}{\frac{V_{DD1}^2}{V_{DD2}^2} P_{gate} \cdot f} = \frac{2 \cdot \frac{5^2}{3.3^2}}{6.5 \cdot 10^{-6} \cdot 80} = 8.8296 \cdot 10^3$$

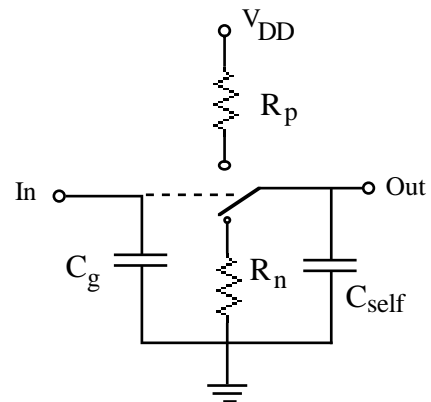
2.4 We have $\tau \approx \frac{4C_L}{\beta} \frac{V_{DD}}{(V_{DD} - |V_T|)^2}$

But τ was about twice too large and we use an RC-model

$$\tau \approx R_x C_{self}$$

for the charge and discharge times. Hence,

$$R_x \approx \frac{2}{\beta} \frac{V_{DD}}{(V_{DD} - |V_{Tx}|)^2}$$



2.5 Determine the largest current through both of the transistors during switching. We have the same current $I_{Dn} = -I_{Dp}$ and gate-source voltage for the n-device is V_m and $(V_m - V_{DD})$ for the p-device, respectively. V_m is the

gate-source voltage when the current is maximum. Since, both devices are in the saturation region we get:

$$\frac{\mu_n C_{ox} W_n}{2 L_n} (V_m - V_{Tn})^2 = \frac{\mu_p C_{ox} W_p}{2 L_p} (V_{DD} - V_m + V_{Tp})^2$$

Solving for V_m we get $V_m = \frac{V_{DD} + V_{Tp} + \sqrt{a} V_{Tn}}{1 + \sqrt{a}}$

where $a = \frac{\mu_n W_n}{\mu_p W_p}$

Now, assume that $a = 1$, i.e., symmetric switching

$$\Rightarrow V_m = \frac{V_{DD} + V_{Tp} + V_{Tn}}{2} = \frac{V_{DD}}{2} \Rightarrow$$

$$\begin{aligned} I_{Dn} &= \frac{\mu_n C_{ox} W_n}{2 L_n} \left(\frac{V_{DD}}{2} - V_{Tn} \right)^2 = \\ &= \frac{(5.6 \cdot 10^{-2})(3.9)(8.85 \cdot 10^{-12})W_n}{(2)(100 \cdot 10^{-10}) L_n} \left(\frac{5}{2} - 0.75 \right)^2 \approx 332 \frac{W_n}{L_n} \quad [\mu A] \end{aligned}$$

where $C_{ox} = \frac{\epsilon_r \epsilon_0}{T_{ox}}$

Rumors has it that the n- and p-transistors in the inverter that drives the global clock in the *Alpha*TM chip (Digital Equipments) has a combined widths of about 10 cm and 14 cm, respectively. The minimum feature size in the CMOS process is a 0.75 μm , but the channel length is 0.5 μm . The chip runs at 200 MHz and consumes about 30 W at 3.3 V. The number of devices is $1.68 \cdot 10^6$ on a 16.8×13.9 mm chip. Current high-performance chips consume 40 to 80 W at 1.8 V.

We guess that $T_{ox} \approx 100 \text{ \AA}$. We have

$$\beta = \frac{\mu_n \epsilon W}{T_{ox} L} = \frac{(5.6 \cdot 10^{-2})(3.9)(8.85 \cdot 10^{-12})W}{(100 \cdot 10^{-10})L} = 193 \cdot 10^{-6} \frac{W}{L} \quad [A]$$

The resulting drain current becomes

$$I_{Dn} \approx 193 \cdot 10^{-6} \frac{10 \cdot 10^{-2}}{0.5 \cdot 10^{-6}} = 38.6 \text{ Amperes}$$

Obviously, it is not possible to have such a large current! Special measures must be employed in order to avoid such large currents.

2.7 Assume that the power supply voltage is $V_{DD1} = 5 \text{ V}$. The power consumption for the one-PE solution is:

$$P_1 = C f V_{DD1}^2$$

where C is the equivalent switched load and f is the switch frequency. Now, using two PEs, the available computation time for each PE is doubled. Hence, the switch frequency can be halved. Assume that the load for each PE increases to $1.1C$ due to the larger circuit area and additional wire routing. The propagation delay may be doubled, hence the power supply voltage can be reduced to

$$\frac{t_{p2}}{t_{p1}} = \frac{\frac{1.1 CV_{DD2}}{(V_{DD2} - V_T)^2}}{\frac{CV_{DD1}}{(V_{DD1} - V_T)^2}} = \frac{1.1 V_{DD2}(V_{DD1} - V_T)^2}{V_{DD1}(V_{DD2} - V_T)^2} = \frac{1.1 V_{DD2}(5 - 0.75)^2}{5(V_{DD2} - 0.75)^2} = 2$$

Solving for V_{DD2} we get

$$19.869 V_{DD2} = 10(V_{DD2}^2 - 1.5 V_{DD2} + 0.5625)$$

$$\text{and } V_{DD2}^2 - 0.486875 V_{DD2} - 0.5625 = 0$$

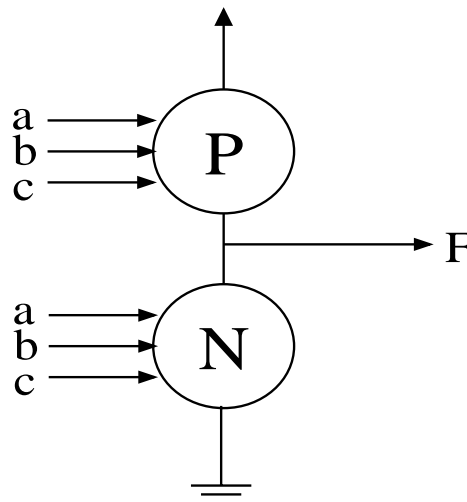
$V_{DD2} = 0.16957 \text{ V}$ or 3.3173 V Hence, $V_{DD2} = 3.3173 \text{ V}$ since the supply voltage must be larger than V_T . The power consumption can be reduced to

$$P_2 = 2.2C \frac{f}{2} V_{DD2}^2 = 2.2 \frac{1}{2} \frac{V_{DD2}^2}{V_{DD1}^2} C f V_{DD1}^2 = 1.1 \frac{3.3173^2}{5^2} P_1$$

$$P_2 = 0.484 P_1$$

Conclusion: It is necessary to reduce the supply voltage when geometry's are scaled down. This reduces the power consumption, but also the speed. Now, the reduction in minimum feature size increases the speed and the number of devices that can be put onto a single chip. Thus, the expected increase in speed will not be as large as was expected from the simple scaling policy that was discussed in section 2.6. It is therefore advantageous to use highly parallel algorithms that can exploit the large number of devices that can be put onto the chip in order to achieve high throughput implementations.

2.8 Static CMOS.



We have $\bar{F} = S_n \Leftrightarrow F = \bar{S}_n$

$$S_n = ab + ac + bc \Rightarrow F = \overline{S_n} = \overline{ab + ac + bc}$$

or

$$F = S_p = (\overline{a + b})(\overline{a + c})(\overline{b + c}) = (\overline{ab})(\overline{ac})(\overline{bc}) = \overline{ab + ac + bc}$$

2.9 Precharge-Evaluation logic.

The circuit is an N-type block. We have $\overline{F} = S_n \Leftrightarrow F = \overline{S_n}$

$$S_n = (b + c)a + bc = ab + ac + bc \Rightarrow F = \overline{S_n} = \overline{ab + ac + bc}$$

- 2.10 The logic transistors in the switch nets will not conduct until the evaluation is completed in the preceding gates. A drawback with this approach is that inverting functions cannot be realized. This logic is called domino logic. Another drawback is charge sharing between internal nodes. This can be solved by precharging the node.