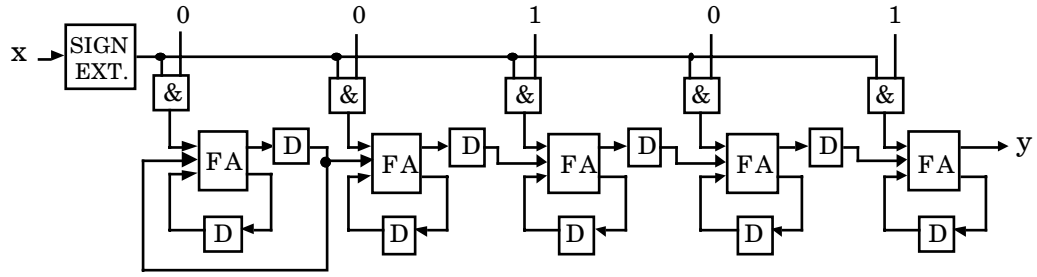
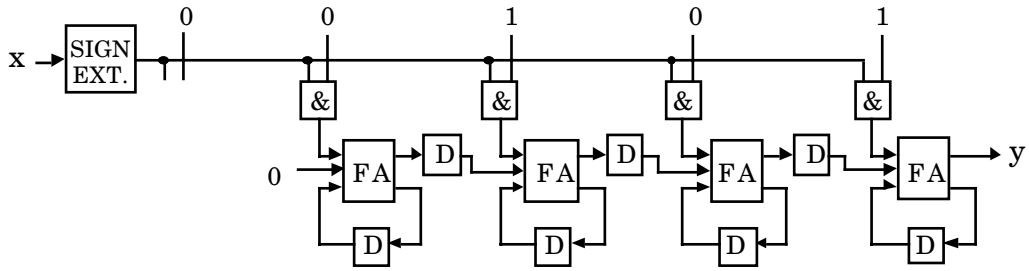
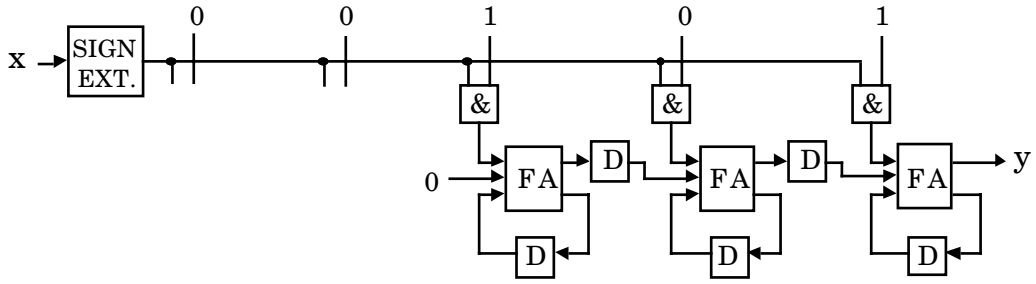
11.5 a) Block diagram for bit-serial multiplier with coefficient $\alpha = (0.0101)_2$ is shown below.



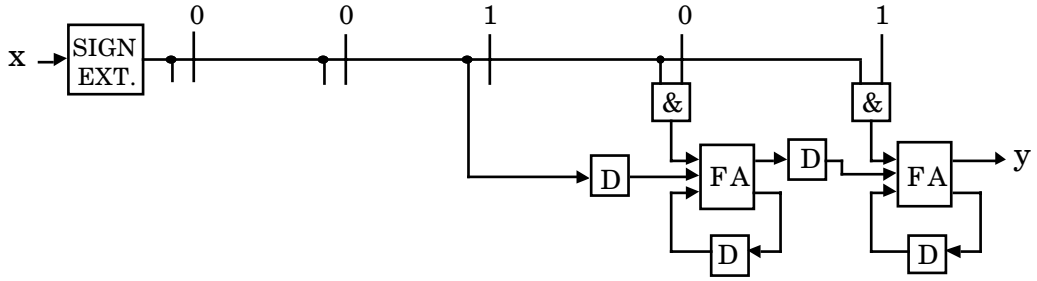
If the most significant bit in the coefficient is 0, then the product for this bit is always 0 and, hence, the result is always 0 or the output from this bit can be replaced with a 0. The resulting block diagram is shown bellow.



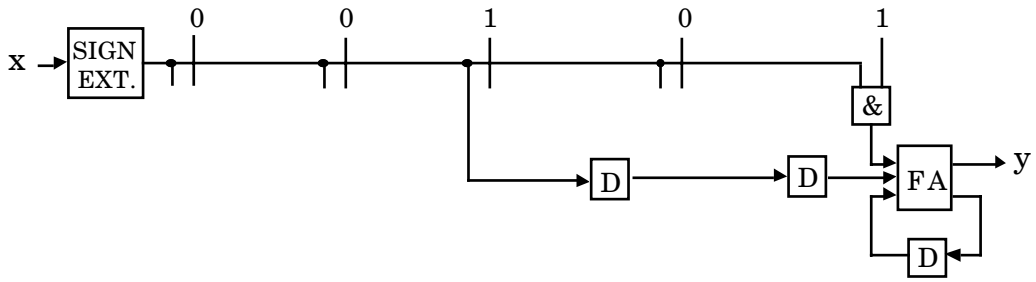
For the same reason, we can simplify the next significant bit and the output signal is 0.



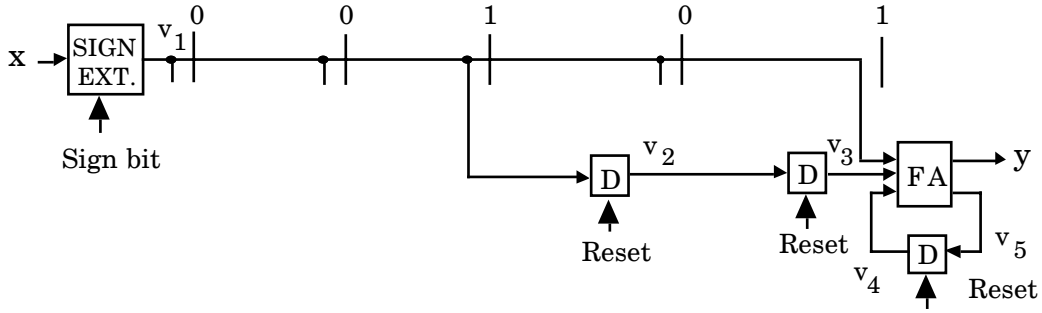
The next significant bit is 1. The output from AND-gate is therefore equal to the input signal *x*. Since the input from the preceding bit is zero and the carry D-flip-flop is reset to 0 at the beginning, the carry output from this bit is 0. The sum for the addition is *x*. Therefore this bit can be replaced with a D-flip-flop.



The coefficient for the next bit is 0, with the reason, the carry and the input is always 0. Therefore we can simplify this bit to a D-flip-flop.



The coefficient at the last significant bit is 1 and should add result from the previous bit. There is no simplification at this bit. The resulting multiplier is shown below.



b) Control signal: assume that the word length is W_d for the data and W_c for the coefficient. Before the computation, all carry D-flip-flops have to reset to 0. The multiplication have to take $W_d + W_c - 1$ clock cycles, where $W_c - 1$ clock cycles are needed for sign extension.

c) A new multiplication can started after $W_d + W_c - 1 = 12 + 5 - 1 = 16$ clock cycles. In some case, one extra clock cycle is required for the reset of all D-flip-flops. This depends on the ways of realization.

d) Verification

x	v1	v2	v3	v4	v5	y	
0	0	0	0	0	0	0	(LSB)
1	1	0	0	0	0	1	
0	0	1	0	0	0	0	
1	1	0	1	0	1	0	
-	1	1	0	1	1	0	
-	1	1	1	1	1	1	
-	1	1	1	1	1	1	
-	1	1	1	1	1	1	(MSB)

X $\alpha = -0.75 \cdot 0.3125 = -0.234375 = (1.1100010)2 = y$