Scaling of electronics

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Outline

Introduction
CMOS Logic
Physical limits to transistors and logic
Physical limits to interconnects
Conclusions

Introduction

Traditional logic techniques has been extremely successful
(Moores law, 2x performance each 18 months, valid >30 years (as yet))

New techniques needed to prolong Moores law ?

Objective:

Review “traditional logic” to put new techniques in perspective

Investigate ultimate limits to “traditional logic”

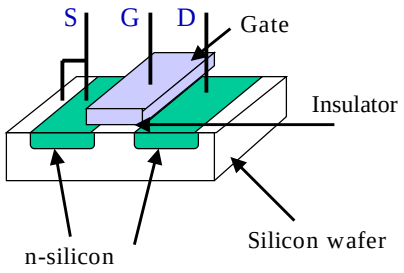
CMOS logic

CMOS will be used as the main example of traditional logic
(Wanless and Sah, 1963)

Key characteristics:
Flexibility (can form an infinite number of logic functions)
Isolation (output does not affect input)
Logic gain (output may drive more than one following gate)
Restoring (Signal quality restored in each gate)
Low cost
Speed
Low power consumption

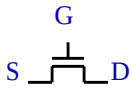
CMOS logic

The n-MOS transistor



Positive gate voltage induces an electron channel

Electron channel conducts between source and drain

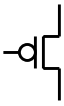


Symbol

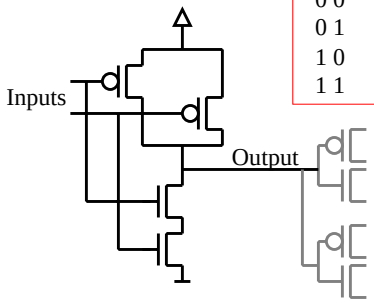
CMOS logic

Basic function

n-MOS, conducting for $V_{GS}>V_T$



p-MOS, conducting for $V_{GS}<-V_T$



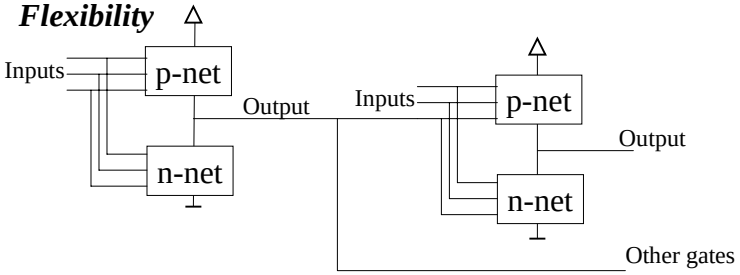
NAND gate

Loading gates

Inputs	Output
0 0	1
0 1	1
1 0	1
1 1	0

CMOS logic

Flexibility



Isolation

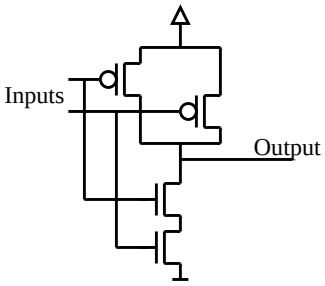
Signals on outputs do not affect inputs

Logic gain

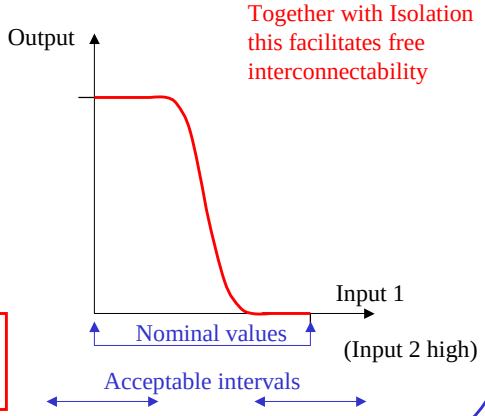
Outputs may drive more than one following gate

CMOS logic

Restoring



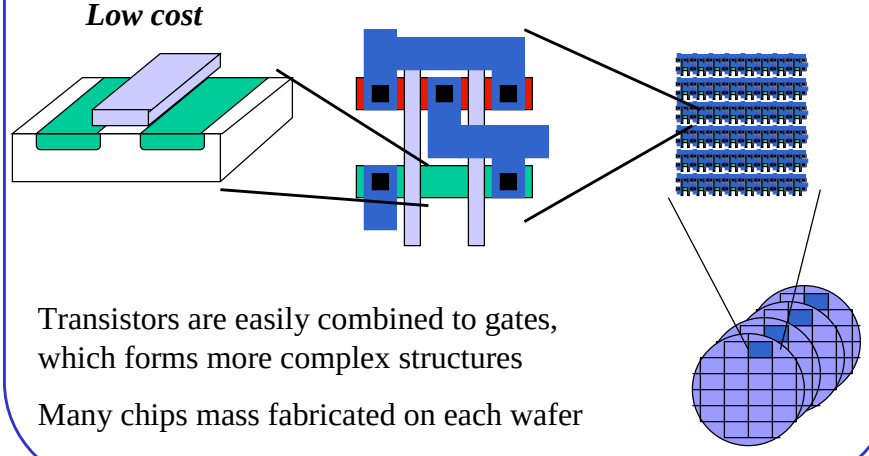
NOTE:
Needs three terminal device with large output impedance



Together with Isolation this facilitates free interconnectability

CMOS logic

Low cost

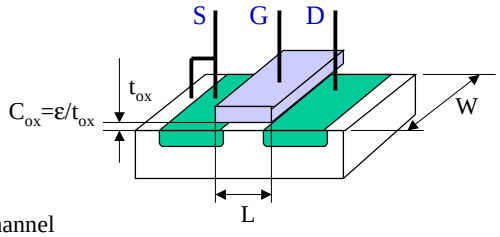


Transistors are easily combined to gates, which forms more complex structures

Many chips mass fabricated on each wafer

CMOS logic

Transistor speed



Short channel model
(M Lundstrom, 1997)

V_D large
Gate voltage induce charge density $q_c=C_{ox}(V_G-V_T)$ in channel
(V_T corresponds to inactive charge and work function differencies)

Electron current $I=qv_{th}W$ is injected from source, v_{th} thermal velocity (~10^5m/s)

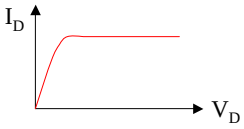
Inherent delay: one transistor discharges the following transistor:

$t_{d0} = Q/I=q_cWL/q_cv_{th}W = L/v_{th}$

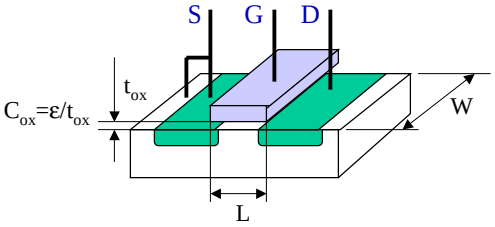
L=0.1µm; $v_{th}=10^5$m/s; t_{d0}=1ps

CMOS logic

Transistor modelling



Short channel model



For any charge vs gate voltage we
may write $I_D=(q_{cs}-q_{cd})v_{th}W=g(V_G)-g(V_G-V_D)$,
where g(x) is any function.
Example: two logical transistors in series, intermediate drain voltage V_{D1}:
$I_D=g(V_{dd})-g(V_{dd}-V_{D1})=g(V_{dd}-V_{D1})$ (<bottom transistor>=<top transistor>)
As a result: $I_D=g(V_{dd})/2$.

CMOS logic

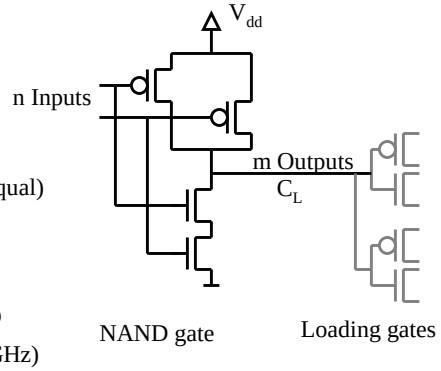
Logic speed

Delay: $t_d = Q/2I_{eff}=C_L *V_{dd}n/2I$
$I_{eff}=I/n$, n serial transistors; $I = qv_{th}W$
$C_L \sim m(1+\gamma)C_{Gn}+C_w$
$\gamma=W_p/W_n$, transistor sizes (n,p currents equal)

$$t_d = \frac{n}{2}\frac{C_L}{C_{Gn}}t_{d0} \qquad C_{Gn} = \frac{q_c WL}{V_{dd}}$$

m=n=2 γ=3 $C_{dn}=C_{gn}$ $C_w=4C_{gn}$ ➔ $t_d=12t_{d0}$

(Clock frequency $f_c<1/4t_d$; 0.1µm $f_c<20$GHz)



CMOS logic

Low power

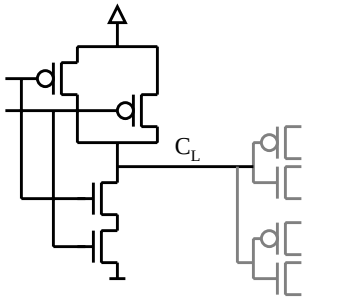
Static power zero
(No current for any static input)

Dynamic power given by

$P=\alpha f_c C_L V_{dd}^2$

For each full logic change,
charge $C_L V_{dd}$ taken from supply

α activity, f_c clock frequency
No activity - no power!



NAND gate

Loading gates

CMOS logic

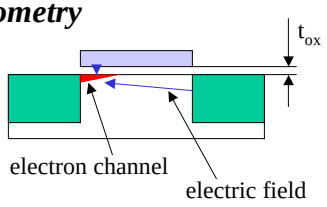
CMOS logic extremely robust:

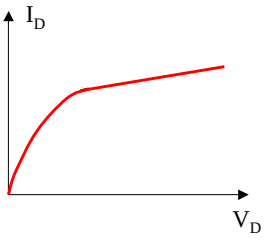
0.1 - 250V supply voltage
4 - 600K operation temperature
0.1-20µm geometry
Facilitates mass produced chips with
100M simultaneously operating transistors.

Robert W Keyes, 2001: ”The failure of any other [than vacuum tube and transistor] compact source of electronic gain to emerge in almost a century of electronics must be regarded as a fundamental limit to device technology”

Physical limits to transistors

Geometry





Gate must shield source from drain field to keep low dI_D/dV_D (to keep large gain)

➔ $L>>t_{ox}$

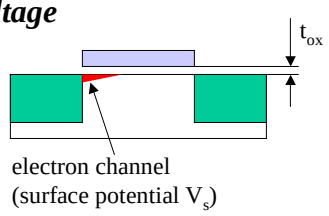
t_{ox}>1.5nm to prevent tunneling leakage (SiO_2 insulator)

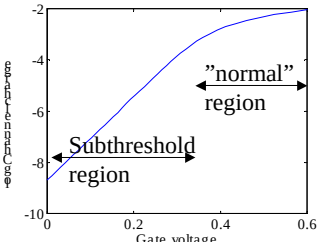
➔ L>15nm (Estimated speed t_{d0}=0.15ps ➔ $f_T=1/2\pi t_{d0}$=1.06THz)

(Experimental: L=30nm; *L may be smaller by surrounding gate*)

Physical limits to transistors

Voltage





Very small voltages (Subthreshold region):

q_c directly controlled by surface potential $q_c = q_{c0}e^{\frac{qV_s}{kT}} = q_{c1}e^{\frac{qV_G}{nkT}}$ $n \approx 1.5$

Drain current $I \propto e^{\frac{qV_G}{nkT}}$

Represents the steepest possible I(V) behaviour ($\frac{1}{I}\frac{\partial I}{\partial V} \le \frac{q}{kT}$ (with n=1))

In order to keep gain >10 in inverter we need V_{dd}>4kT (0.1V)

Physical limits to transistors

Noise

Output node has a noise voltage of $v_n^2=kT/C_L$ (voltage variance)
(Thermal noise in transistor channels at bandwidth given by channels and capacitor)

System error probability rate:
(probability that noise exceeds $V_{dd}/2$)

$$P_{err} = Nf_c erfc\left(\frac{V_{dd}}{2v_n}\right)$$

N number of registers
f_c clock frequency

Assume P_{err} < 1/year; $N=10^8$; f_c=30GHz ➔ $erfc\left(\frac{V_{dd}}{2v_n}\right)=1.1\bullet10^{-26}$ (argument=7.56)

With $\frac{V_{dd}^2}{4v_n^2}=\frac{C_L V_{dd}^2}{4kT}$ we get the a minimum stored energy $C_L V_{dd}^2=1.3\ 10^{-19}J=0.8eV$

Physical limits to transistors

The minimum gate

2-input, 2-output static CMOS gate with n-transisor L=15nm, W=30nm, t_{ox}=1.5nm

$$C_{Gn} \approx \frac{3.4\bullet10^{-11}\, L/2\, W}{w_{ox}} = 5aF$$

$C_L=4*C_{Gn}=20aF$

$V_{dd}=0.1V$ $CV_{dd}^2=2\ 10^{-19}J=1.25eV$ (close to noise limit!)

number of electrons: 12 (close to single electron!)

Physical limits to interconnects

Electrical conductors have two limitations:

Signal velocity limited by velocity of light, (narrow wires worse; RC-limited) $c = \frac{c_0}{\sqrt{\varepsilon}}$

Data rate limited by resistance, (A=metal cross section, L=wire length) $B \approx B_0(\rho, \varepsilon, Z_0)\frac{A}{L^2}$

Wire limitations needs consideration, but is not a severe limitation to electronics inside chip or circuit board

(See C. Svensson, "Electrical interconnects revitalized", www.ifm.liu.se/~Christer/InterconnectManuscript.pdf)

Conclusions

Simple arguments can be used for understanding and predicting logic performance

Several key properties facilitates the ever-increasing complexity of CMOS logic

We are very far from fundamental limits today

- Moores law may be valid 20 years more (10000x increased performance)
- CMOS may approach fundamental physical limits
- These limits are most probably valid for any electronics-like system

References

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