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On Analog Power Consumption

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Outline

Introduction
Basics of analog power consumption
Comparison analog and digital
RF elements
Example RF frontend
Example ADC
Conclusions

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Introduction

Analog power consumption is complex and badly understood

Text books and practice specialize on performance constraints rather than power

This is an attempt to address analog design for low power and to define lower bounds to analog power consumption

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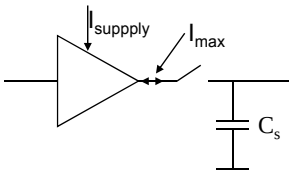
Basics of analog power consumption

Ideal sampler



Noise voltage generated: $v_{nS}^2 = \frac{kT}{C_s}$

Maximum sine voltage with supply voltage V_{FS}:

$v_s^2 = \frac{V_{FS}^2}{8}$ Gives dynamic range: $DR = \frac{v_s^2}{v_{nS}^2} = \frac{V_{FS}^2 C_s}{8kT}$

or, capacitance needed: $C_S = \frac{8kTDR}{V_{FS}^2}$

To drive the capacitor we need a current of $I=C_s V_{FS} 2f_s$,

leading to a power consumption of $P_S = IV_{FS} = 16kTf_s DR$

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Basics of analog power consumption

Ideal sampler

$$P_S = IV_{FS} = 16kTf_sDR$$

This expression is valid for any switched capacitor circuit
(Example a first order switched capacitor filter)
First described by Vittoz 1990.

Note that this expression is *independent of technology*

Note that this expression is *independent of supply voltage (but assumed V_{FS}=V_{dd}; V_{dd} is supply voltage)*

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Basics of analog power consumption

Ideal sampler - impact of technology

In the above derivation we used $C_S = \frac{8kTDR}{V_{FS}^2}$

But C_s can not be made smaller than the smallest capacitance of the actual technology, C_{min}.

So actually we should use C=max(C_s, C_{min}) in power estimation.

In the following we use the input capacitance of a minimum inverter as C_{min}. C_{min}=4*C_{gn}. C_{gn} will scale with technology as the feature size (half feature size - half capacitance)

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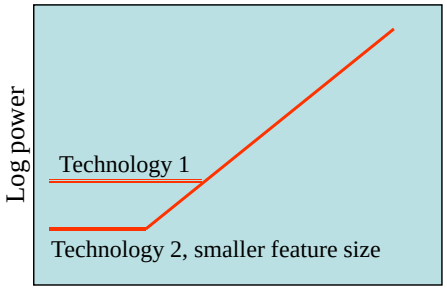
Basics of analog power consumption

Ideal sampler - impact of technology

Large DR - independent technology

Smaller DR - technology dependent
Smaller feature size - less power

Note, scaled as (feature size)^3
($P_S \sim V_{FS}^2 C_{min}$)



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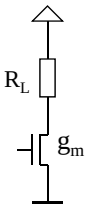
Basics of analog power consumption

The transistor



Drain noise current: $i_{nD}^2 = 4kT\gamma g_m B$

Equivalent input noise: $v_{nG}^2 = 4kT\gamma \frac{1}{g_m} B$

Dynamic range: $DR = \frac{V_{FS}^2}{8} \frac{g_m}{4kT\gamma B}$

Required g_m for dynamic range DR: $g_m = \frac{32kT\gamma B}{V_{FS}^2} DR$

Required drain current: $I_D = g_m V_{eff}$

Power consumption: $P = IV_{FS} = 32kT\gamma B \frac{V_{eff}}{V_{FS}} DR$ (compare $P_S = 16kTf_s DR$)

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Basics of analog power consumption

The transistor – a note on V_{eff} and γ

V_{eff} definition: $V_{eff}=I_D/g_m$ γ defined from noise measurements

Bipolar transistor: $V_{eff}=kT/q$ $\gamma=1/2$ (shot noise)

Long channel MOST: $V_{eff}=(V_G-V_T)/2$ $\gamma=2/3$ (resistance noise)

Long channel MOST in subthreshold: $V_{eff}=mkT/q$, m=1.2…1.5

Submicron MOST: V_{eff} in transition region γ~1.5-2

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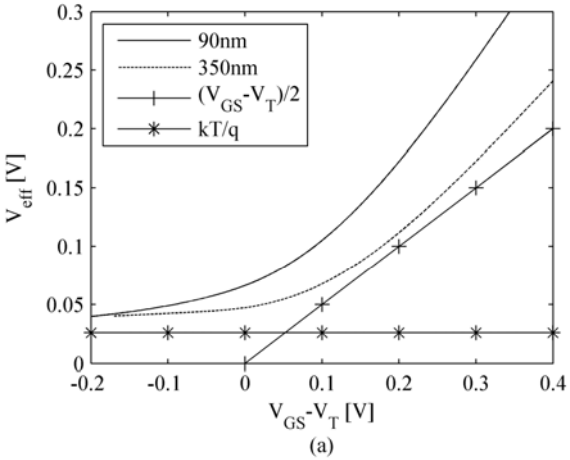

V_{eff} vs V_G for
a 90nm process
a 350 nm process

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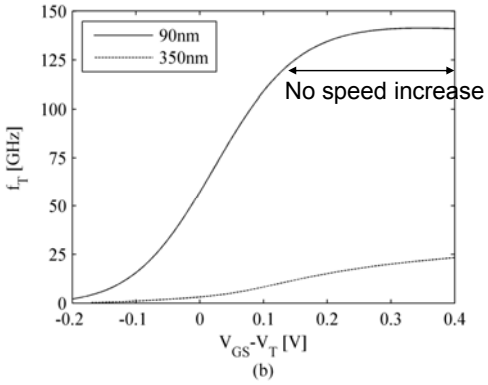
The transistor – a note on V_{eff} and speed.

Speed controlled by f_T

$f_T=g_m/2\pi C_g$



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The transistor – a note on V_{eff} and input swing

For a linear transistor behaviour we expect a limited drain current variation, say $I_{DC} \pm \Delta I_d = I_{DC} \pm I_{DC}/2$, with $I_{DC}=g_m V_{eff}$.

We then have $\Delta V_g=\Delta i_d/g_m=V_{eff}/2$, or $V_{FSin}=2\Delta V_g=V_{eff}$

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Basics of analog power consumption

The transistor – a note on V_{dd}

We assumed supply voltage = V_{FS}

With higher supply, V_{dd}, we define voltage efficiency $\eta_v = V_{FS}/V_{dd}$

Then power *increases* by $1/\eta_v$

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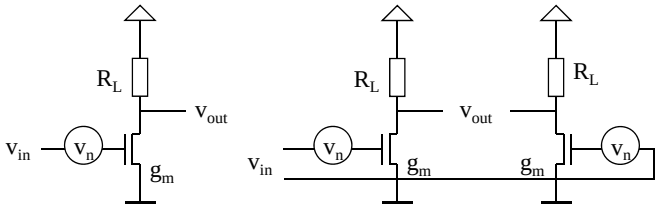
Basics of analog power consumption

The transistor – a note on differential circuits



Same transistors, same bias, same signal per transistor

$$DR_{diff} = \frac{(2v_{in})^2}{2v_n^2} = 2DR_{SE} \quad P_{diff} = 2P_{SE}$$

Same dynamic range
Same power

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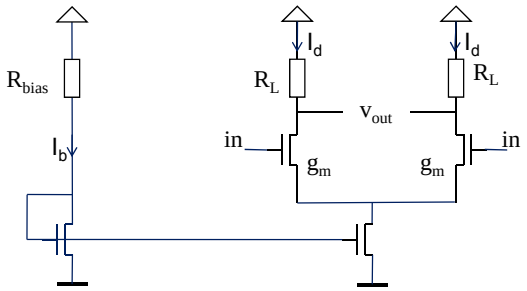
Basics of analog power consumption

The transistor – a note on bias circuits



Current efficiency, $\eta_I = 2I_d/(I_b+2I_d)$. Note, I_b may need to be large for eg. low noise

Note – bias circuit may be shared

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Basics of analog power consumption

The transistor – impact of technology

Regarding minimum g_m.
We can always reduce g_m to adapt to DR by reducing V_G.
BUT this leads to small V_{eff}, which may limit speed or input swing
Maybe we will have g_{mmin} and I_{DCmin}.

Power proportional to V_{eff}/V_{FS}

Classical CMOS, this relation was kept constant
V_{FS} (V_{dd}), V_G and V_T scaled with process scaling
Submicron CMOS, V_{eff} is reduced very slowly.
So power may *increase* with reduced supply voltage! (Annema et. al.)

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Basics of analog power consumption

The transistor – a conclusion

A transistor amplifier (single ended or differential) uses power:

$$P = IV_{FS} = 32kT\gamma B\frac{V_{eff}}{V_{FS}}DR$$

This is constrained by:

Increased by $1/\eta_v$ for $V_{FS}<V_{dd}$
Increased by $1/\eta_i$ for extra currents (eg. bias)
V_{eff} must be large enough for transistor speed ($f_T=g_m/2\pi C_g$ large enough)
V_{eff} must exceed input swing, V_{FSin}
Technology dependence at low DR - complex

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Basics of analog power consumption

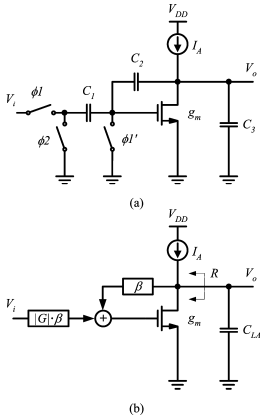
A switched C amplifier

Input data sampled during Φ1
Output data generated (and sampled by following stage) during Φ2

Nominal gain, $G=-C_1/C_2$
Return factor $\beta=C_2/(C_1+C_2)$

Output resistance $R=1/\beta g_m=(1+|G|)/g_m$

Output capacitance, $C_{LA}=C_1C_2/(C_1+C_2)+C_3$



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Basics of analog power consumption

A switched C amplifier

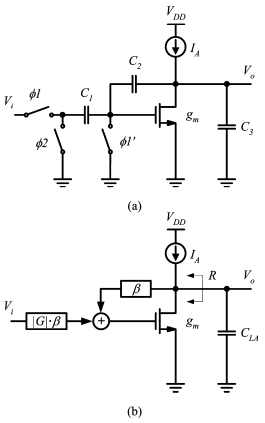
Output noise voltage:

$$\overline{v_o^2} = 4kT\gamma g_m R^2 \cdot \frac{1}{4RC_{LA}} = \frac{kT}{C_{LA}} \cdot \gamma \cdot (1+|G|).$$

Requiring a dynamic range of $DR=V_{FS}^2/v_o^2$:

$$C_{LAn} = 8kT\gamma(1+|G|)\frac{DR}{V_{FS}^2}.$$

This gives a requirement on capacitance (similar to kT/C requirement)



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Basics of analog power consumption

A switched C amplifier

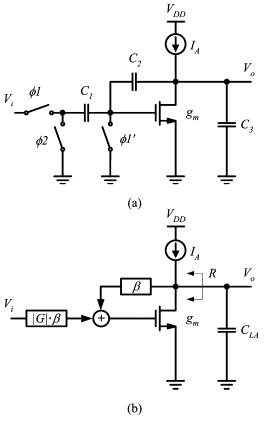
We have further a speed requirement
Time constant of circuit is $\tau=RC= (1+|G|)C_{LA}/g_m$

τ must be small enough for settling to an accuracy of $1/\sqrt{DR}$ within T_{se}:

$$\tau = \frac{2T_{se}}{\ln(DR)}$$

This gives a requirement on g_m and therefore on I_{DC}

$$I_{DC} = \frac{C_{LA}V_{eff}(1+|G|)\ln(DR)}{2T_{se}}$$



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Basics of analog power consumption

A switched C amplifier

We may refine the speed requirement by also considering slewing. With I_{DC} we get a slewing time of:

$$T_{sl} = \frac{C_{LA} V_{FS}}{I_{DC}}$$

So, totally we need $T_{se}+T_{sl}=1/2f_s$ for slewing+settling leading to I_{DC}. From this we estimate total power:

$$P_{DC} = I_{DC} V_{dd} = \frac{I_{DC} V_{FS}}{\eta_v} = \left(1 + \frac{V_{eff}\left(1+|G|\right)\ln(DR)}{2V_{FS}}\right)\frac{2C_{LA}V_{FS}^2 f_s}{\eta_v}$$

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Basics of analog power consumption

A switched C amplifier

$$P_{DC} = I_{DC} V_{dd} = \frac{I_{DC} V_{FS}}{\eta_v} = \left(1 + \frac{V_{eff}\left(1+|G|\right)\ln(DR)}{2V_{FS}}\right)\frac{2C_{LA}V_{FS}^2 f_s}{\eta_v}$$

Note that the slewing term corresponds to the “ideal” sampling power

In this case we may allow $V_{eff}<V_{FS}$; if transistor is shut off, there is slewing

Note that again power is proportional to the capacitance, C_{LA}

Capacitance controlled by dynamic range (noise level) and more…

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A switched C amplifier – impact of technology

For small DR C_{LAn} may be smaller than C_{min}. Then it must be replaced by C_{min}.

$C_{LA}=\max(C_{LAn}, C_{min})$

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Basics of analog power consumption

A switched C amplifier – impact of mismatch

Sometimes we need to consider accuracy because of mismatch. Eg. we need to reproduce G within a certain accuracy, say $\Delta G/G$, corresponding to, say, a relative variance of G, σ_G, $3\sigma_G=\Delta G/G$.

As G depends on two capacitors, we may estimate $\sigma_G=\sqrt{2}\sigma_C$, where σ_C is the process spread of capacitances. With capacitor area A we have:

$$\sigma_C=\frac{K_\sigma}{\sqrt{A}} \qquad C=K_C A$$

with typical K_σ=1%μm and K_C=1fF/μm² (90…350nm processes). Thus we need the capacitor to be larger than

$$C_{LAm}=\frac{2K_C K_\sigma^2}{\sigma_G^2}=\frac{2K_C K_\sigma^2}{9}\left(\frac{\Delta G}{G}\right)^{-2}$$

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Basics of analog power consumption

A switched C amplifier – impact of mismatch

An interesting observation: C_{LAn} proportional to DR/V_{FS}^2
C_{LAm} proportional to DR

Traditionally mismatch limitations are considered worse than noise limitations

With our formulas we find that their effects will be similar around V_{FS}=1V
So, mismatch less important for deep submicron processes?

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Basics of analog power consumption

A switched C amplifier – design scheme

1. **Decide on capacitance, C_{LA}=max(C_{LAn}, C_{min}, C_{LAm})**
   Controlled by DR, technology, and accuracy
2. **Decide on speed; calculate g_m**
3. **Decide on V_{eff}**
   Depends on speed and swing, leads to I_{DC}
4. **Finish design, estimate power.**

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Basics of digital power consumption

Comparison to analog

Consider a single pole filter / 1-tap FIR filter

Analog, use transistor formula: (with DR=3●2^{2n}/2; B=f_s/2)

$$P_a = 24kT\gamma \frac{V_{eff}}{V_{FS}} f_s 2^{2n}$$

Digital. Need 1 m-coefficient, n-bit multiplier plus 1 n-bit adder
Multiplier uses m adders; 1 adder use n FAs (full adders); each FA uses equivalent 9 inverters, ie. C=9C_{min}. Totally 9(m+1)nC_{min},
With m=6 we have 63nC_{min}.

$$P_d = \frac{1}{2}\alpha f_c 63nC_{\min}V_{dd}^2$$

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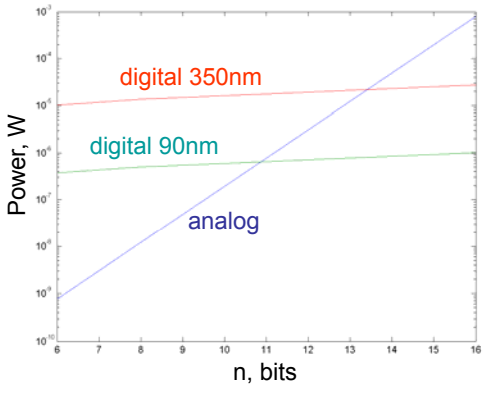
Basics of digital power consumption

Comparison to analog

f_s=20MHz
γ=1.5
V_{eff}=0.1V_{FS}

90nm: V_{dd}=1V
C_{min}=1fF
α=0.1

350nm V_{dd}=3V
C_{min}=3fF
α=0.1



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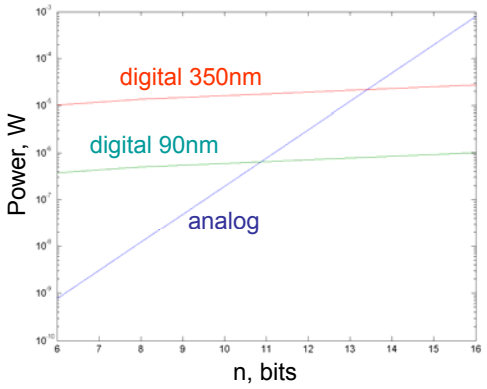
Basics of digital power consumption

Comparison to analog

Analog preferred for low DR

Digital preferred for large DR

Digital improved by scaling



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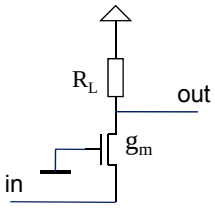
RF elements

The LNA

Normally we need wideband input matching and low noise figure. A good compromise is the common gate stage.



Matching: $R_{in}=1/g_m=R_s$ (R_s - source resistance)

Noise figure: $NF=1+\gamma$

Power consumption: $P=I_D V_{dd}=g_m V_{eff} V_{dd}=V_{eff} V_{dd}/R_s$

given by R_s (normally 50Ω) and V_{eff} (chosen as small as allowed from speed and input swing requirement). Typically I_D=2mA

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RF elements

The LNA – impedance transformation

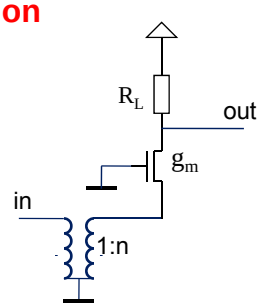
With a transformer, we may transform the source impedance to n^2R_s thus reducing g_m and power consumption by n^2.

Limitations:

For large impedances, induced gate noise will impact – optimum impedance

Transformers not good at high frequencies
- need tuning elements, narrow bandwidth

Transformers replaced by impedance transforming matching network
- need tuning elements, narrow bandwidth



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The LNA – current reuse, high linearity

Matching: $R_{in}=1/(g_{m1}+g_{m2})=R_s$
(R_s - source resistance)

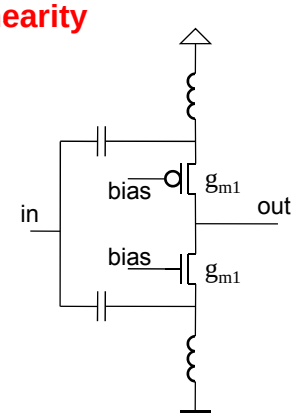
Noise figure: NF=1+γ

Power consumption ($g_{m1}=g_{m2}$, V_{eff} same):
$P=I_DV_{dd}=g_{m1}V_{eff}V_{dd}=V_{eff}V_{dd}/2R_s$

Half power, same supply current used twice.

Inverter-like structure, can be very linear (nonlinearities of n- and p-transistors cancel)

Note, for large input swing, large V_{eff}



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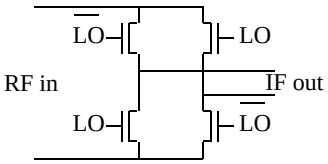
RF elements

Mixers - passive mixer

A passive mixer has zero power consumption

Also, can have reasonably good noise figure

Also, has very low 1/f noise



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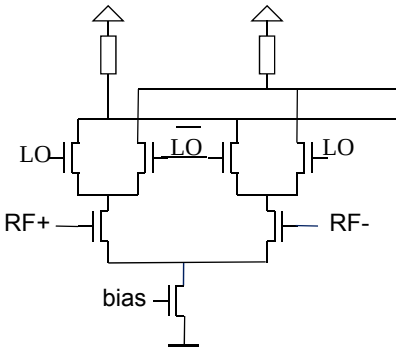
Mixers - active mixer

An active mixer has gain and use power

Similar to LNA design.
Choose g_m for noise (and/or gain)
Adjust V_{eff} to speed or V_{FSin}



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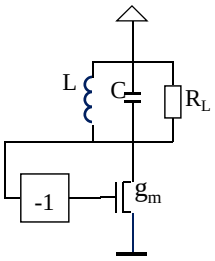
RF elements

VCOs

The VCO, voltage controlled oscillator, is central in a radio. Key performance factor is phase noise.

We use a simple oscillator model, signal and noise is generated by the transistor noise current (The "-1" block can be a transformer or another transistor stage)



Output voltage: $v_o^2 = \left|\frac{Z_L}{1-g_m Z_L}\right|^2 i_n^2 = \frac{R_L^2\omega_0^2}{4Q^2\Delta\omega^2} i_n^2$

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RF elements

VCOs

Noise current: $i_n^2 = 4kT\gamma g_m$

Output power: $P_o = \frac{V_{FS}^2}{8R_L}$

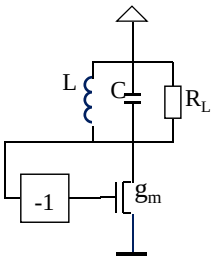
Relative noise spectral density:

$$S(\omega) = \frac{v_0^2}{R_L P_o} = \frac{\gamma kT\omega_0^2}{Q^2 P_o \Delta\omega^2}$$

Thermal energy

Half is phase noise: $L(\omega) = \frac{\gamma kT\omega_0^2}{2Q^2 P_o \Delta\omega^2}$

Stored energy



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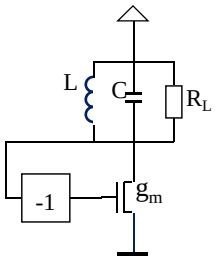
RF elements

VCOs

Power consumption, $P_{DC}=I_{DC}V_{dd}$
$I_{DC}=g_mV_{eff}$, $g_m=1/R_L$, $V_{eff}=V_{FS}$, $V_{dd}=V_{FS}/\eta_v$



We can then estimate the power consumption:

$$P_{DC}=\frac{4\gamma kT}{\eta_v Q^2 L(\omega)\left(\frac{\Delta\omega}{\omega_0}\right)^2}$$

Typical requirement $L(\omega)$=-100dBc/Hz at $\Delta\omega$=100kHz and ω_0=1GHz, with η_v=0.5, γ=1.5, Q=5 (loaded Q) we have P_{DC}=1.2mW

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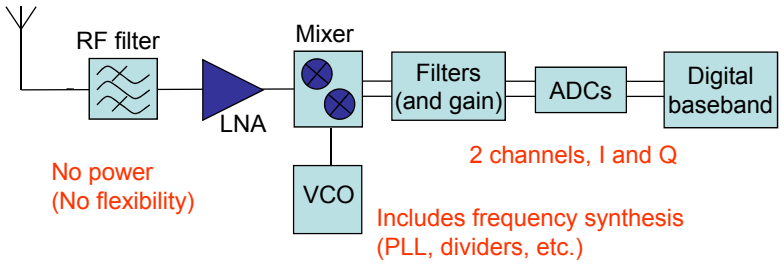
Example RF receiver frontend



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Example RF receiver frontend

	Requirements	Current	Real example
LNA	R_s=50Ω, NF=4dB	2mA	7-12mA
Mixer	Active	(2X2mA)	2X5-12mA
VCO	L(ω)=100dBc/Hz @ 100kHz 1.8-6GHz	3-36mA	4-10mA
IF	4th order; BW=0.35-20MHz	2X9.2mA	2X10mA

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Example RF receiver frontend

Real case: IMEC receiver (Craninckx, et.al., ISSCC 2007), 1.2V supply

Assumptions:
Blocker level -18dBm (corresponds to IIP3=-9dBm)
4th order IF filter created by a 4 stage amplifier

In addition to the above blocks, Real case includes VGA, LO buffer,
PLL divider and phase detector, increasing minimum power from 41 to 65mA

In conclusion, a low power receiver design is close to our estimations

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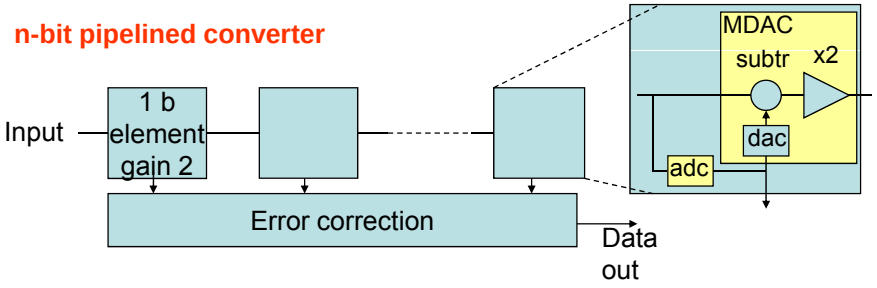
Example ADC

n-bit pipelined converter



By introducing redundancy in each element (eg. 2b adc/dac) it is possible to remove offsets and correct gain errors. Then we do not need to consider accuracy.

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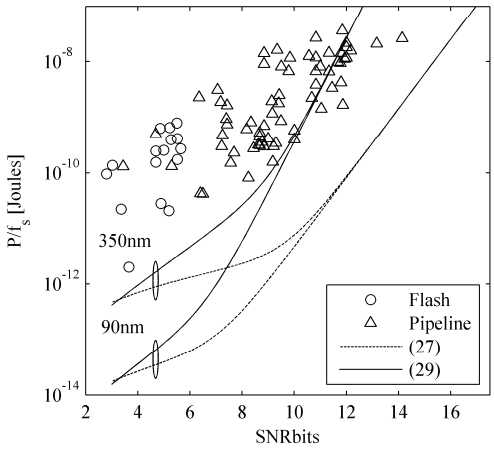
Example ADC



Plot of minimum ADC power for two processes

"(27)" this theory pipelined ADC
"(29)", theory flash ADC

Two processes, 90nm and 350nm (V_{dd}=1V, V_{eff}=100mV, C_{min}=1fF, V_{dd}=3V, V_{eff}=300mV, C_{min}=3fF)

Triangles, experimental pipelined
Circles, experimental flash

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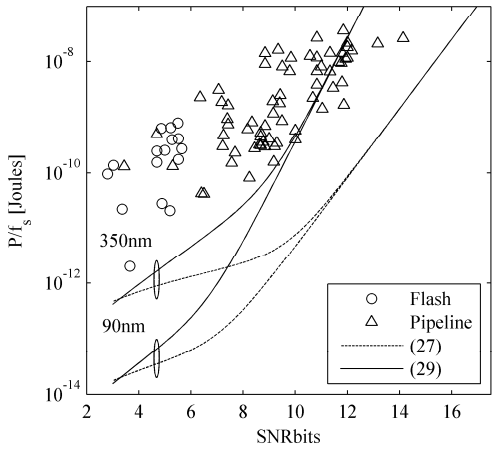
Example ADC



Note1:

High resolution, noise limited
Low resolution, process limited

Note2:

High resolution, experimental approaches theory (10x difference)

Low resolution, larger discrepance (larger development potential)

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Example ADC

Commercial examples

LTC2209, 16b, 160MS/s 1.45W

Our formula: 0.6W **VERY** close (very well developed technology)

ADC083000, 8b, 3GS/s, 1.8W

Our formula (pipe): 0.13mW, much to improve!

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Conclusions

Power consumption in analog parts can be addressed

Smart choices of architecture, circuit topology, and parameters can save power

For large dynamic range, digital often use less power
More so in scaled technologies
Move functions to digital
Perform digital correction of analog parts to save analog power

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