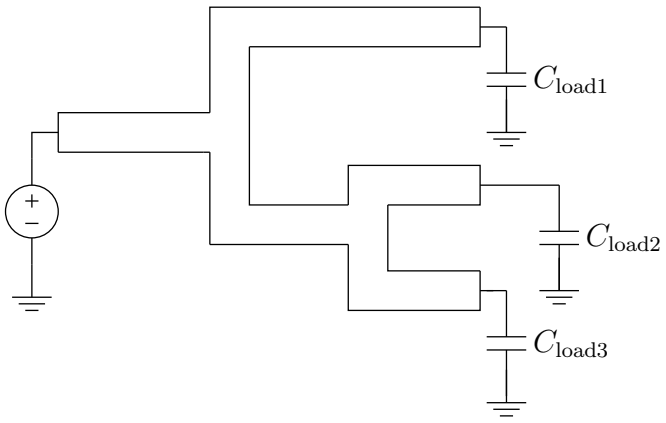
Additional problem for homework assignment #5

We consider the problem of sizing the interconnecting wires of the simple circuit shown below, in which one voltage source drives three different capacitive loads C_{load1}, C_{load2}, and C_{load3}.

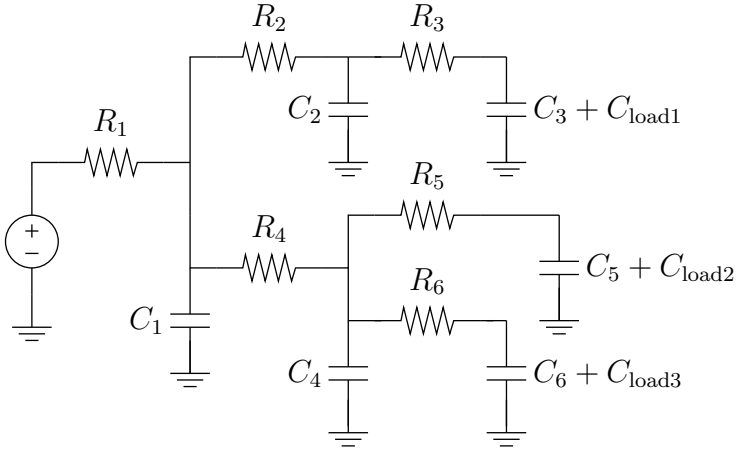


We divide the wires into 6 segments of fixed length l_i; the optimization variables will be the widths w_i of the segments. (The height of the wires is related to the particular IC technology process, and is fixed.) We take the lengths l_i to be one, for simplicity.

Each of the wire segments is modeled by a simple RC circuit, with the resistance inversely proportional to the width of the segment and the capacitance proportional to the width. (A far better model uses an extra constant term in the capacitance, but this complicates the equations.) The capacitance and resistance of the ith segment is thus

$$C_i = k_0 w_i, \qquad R_i = \rho / w_i,$$

where k_0 and ρ are positive constants, which we take to be one for simplicity. We also have $C_{\text{load1}} = 1.5$, $C_{\text{load2}} = 1$, and $C_{\text{load3}} = 5$. Using the RC model for the wire segments yields the circuit shown below.



We are interested in the trade-off between area and delay. The total area used by the wires is, of course,

$$A = \sum_{i=1}^{6} w_i l_i = \sum_{i=1}^{6} w_i.$$

We will use the Elmore delay to model the delay from the source to each of the loads. The Elmore delays to loads 1, 2, and 3 are defined as

$$\begin{aligned}
T_1 &= (C_3 + C_{\text{load1}})(R_1 + R_2 + R_3) + C_2(R_1 + R_2) \\
&\quad + (C_1 + C_4 + C_5 + C_6 + C_{\text{load2}} + C_{\text{load3}})R_1 \\
T_2 &= (C_5 + C_{\text{load2}})(R_1 + R_4 + R_5) + C_4(R_1 + R_4) \\
&\quad + (C_6 + C_{\text{load3}})(R_1 + R_4) + (C_1 + C_2 + C_3 + C_{\text{load1}})R_1 \\
T_3 &= (C_6 + C_{\text{load3}})(R_1 + R_4 + R_6) + C_4(R_1 + R_4) \\
&\quad + (C_1 + C_2 + C_3 + C_{\text{load1}})R_1 + (C_5 + C_{\text{load2}})(R_1 + R_4).
\end{aligned}$$

Our main interest is in the maximum of these delays,

$$T = \max\{T_1, T_2, T_3\}.$$

We also impose minimum and maximum allowable values for the wire widths:

$$W_{\text{min}} \leq w_i \leq W_{\text{max}}.$$

For our specific problem, we take $W_{\text{min}} = 0.1$ and $W_{\text{max}} = 10$.

We compare two choices of wire widths.

1. *Equal wire widths.* Plot the values of area A versus delay T, obtained if you take equal wire widths (varying between W_{min} and W_{max}). You can use the function `elm_del_example.m` on the course website to evaluate the three delays, given the widths of the wires.

2. *Optimal wire widths.* Explain how to find the optimal trade-off curve between area A and delay T, via geometric programming. For the specific problem parameters given, plot the area-delay trade-off curve, using the MOSEK GP solver `mksgpopt`. Compare the optimal trade-off curve with the one obtained in part 1.