High bandwidth, Low Latency Global Interconnect

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Outline

- Introduction
- Modeling transmission lines
- Wire performance
- Network-on-chip example
- Conclusion

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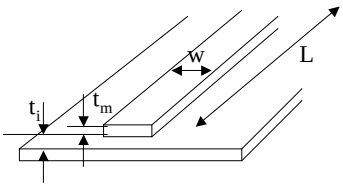
Introduction

Electrical interconnects are considered to be *the* major limitation to performance of scaled electronics.



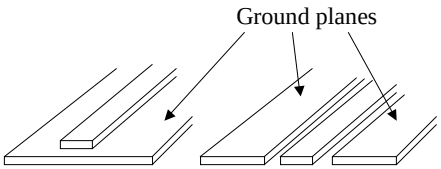
Wire delay ~ RC

$$RC = \frac{\rho L}{t_m w}\frac{\varepsilon w L}{t_i} = \rho\varepsilon\frac{L^2}{t_m t_i}$$

Wire delay scales as (feature size)$^{-2}$
Logic delay scales as (feature size)

Introduction

If properly dimensioned, wires behave as transmission lines.



Microstrip Coplanar waveguide

Wire delay ~ L/v_d

$v_d = v_0/n$

($n = \sqrt{\varepsilon_r}$, refractive index)

Global wires **not** scaled, use upper level metals
Wire delays related to speed of light

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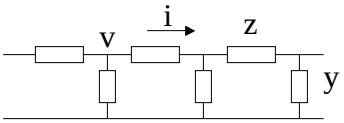
Modeling transmission lines

Lumped wire model:



z,y impedance and admittance per unit length

$$v = Hv(0) \qquad H = e^{\pm\sqrt{zy}x} \qquad i = \frac{v}{Z_c} \qquad Z_c = \sqrt{\frac{z}{y}}$$

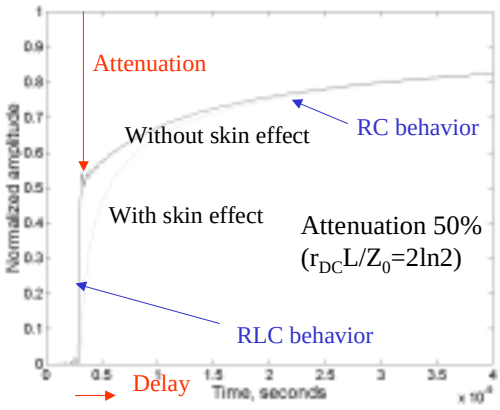
Interpretation: One wave in each direction

In our case, with skin effect:

$$z = j\omega l + r = j\omega l + r_{DC} + r_s(1+j)\sqrt{\omega} \qquad y = j\omega C$$

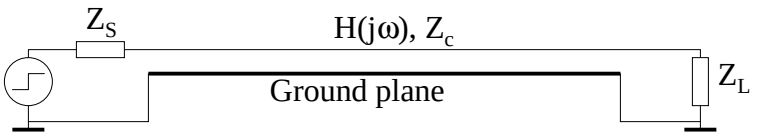
Step response

Step response of *transfer function* H



Attenuation <50% → transmission line behavior

Modeling transmission lines



(Solve circuit equations with two waves)

$$G(\omega)=\frac{2Z_L H}{Z_L\left(\left(1+H^2\right)+\frac{Z_S}{Z_c}\left(1-H^2\right)\right)+Z_C\left(\left(1-H^2\right)+\frac{Z_S}{Z_c}\left(1+H^2\right)\right)}$$

For $Z_s=Z_L=Z_c$: G=H

For $Z_s=Z_c$, $Z_L=\infty$: 2H

(Note that Z_c depends on ω)

$(\omega\to\infty,\ Z_c \to Z_0=\sqrt{l/c})$

Modeling transmission lines

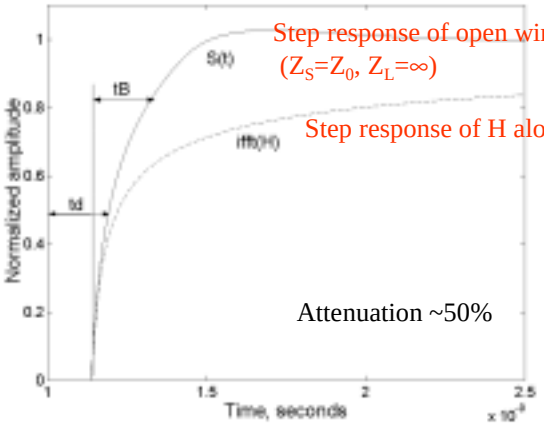
Converting to time domain

$H = e^{-\sqrt{(j\omega l+r)j\omega c}x}$ Voltage transfer function
Complex and frequency dependent r

$s = \frac{1}{2}\left(1+erf\left(a_1\left(t-t_1\right)\right)\right)$ (Step response in time domain)

$v(t) = ifft(HS)$ (Step in time domain)

Modeling transmission lines



Note:
Full step response better than H alone

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Wire performance

Latency (delay)

High loss case (RC-case), $r_{DC}L/Z_0>2\ln 2$. Elmore delay good approximation:

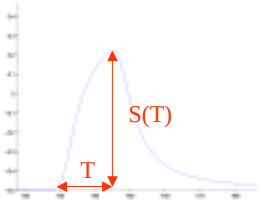
$$t_d = \left(R_S\left(C_S + C_w + C_L\right) + R_w\left(\frac{C_w}{2} + C_L\right)\right)\ln 2 \qquad Z_S = R_S \quad Z_L = \frac{1}{sC_L}$$

Low loss case (LC-case), $r_{DC}L/Z_0<2\ln 2$:

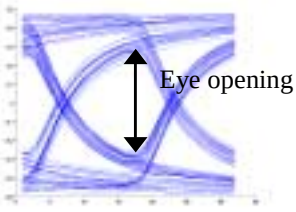
$$t_d = \frac{L}{v_d} = \frac{L}{v_0/\sqrt{\varepsilon_r}}$$

Wire performance

Capacity or maximum data rate



Single pulse

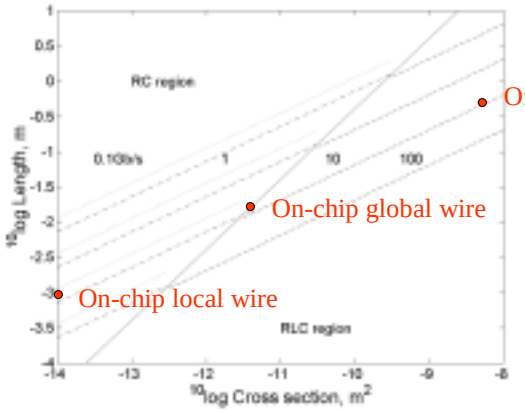


Eye diagram

Eye opening = 2S(T)-1, S(t) step response, T symbol time

We need a minimum opening for safe data detection, say 64%

Wire performance



Off-chip wire (board)

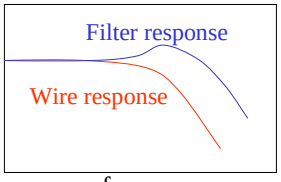
On-chip global wire

On-chip local wire

Wire performance

Pre-emphasis

Pre-emphasis is a standard method to increase the data-rate by "sharpening" the step response



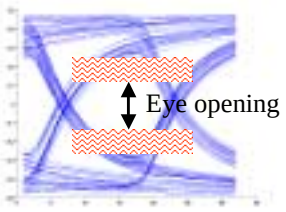
The open-wire response shows "self-pre-emphasis" because of frequency-dependent Z_c

Pre-emphasis is further enhanced by "overdriving", using $R_S<Z_0$

Wire performance

Crosstalk

Neighboring wires cause crosstalk, which further reduces the eye-opening



64% eyeopening without crosstalk, plus 18% crosstalk leaves 46% eyeopening

Crosstalk is a complex function of mutual inductance and capacitance (function of wire spacing), signal risetime, and driver and load impedances. We simulated it using HSPICE (and two neighboring wires).

Wire performance

Power consumption

For “short”, open wires (electrical length < half symbol time) (1cm length at 10Gb/s):

$$P = \frac{1}{4} B C_w V_{dd}^2$$

B, datarate, V_{dd}, voltage swing, data assumed random

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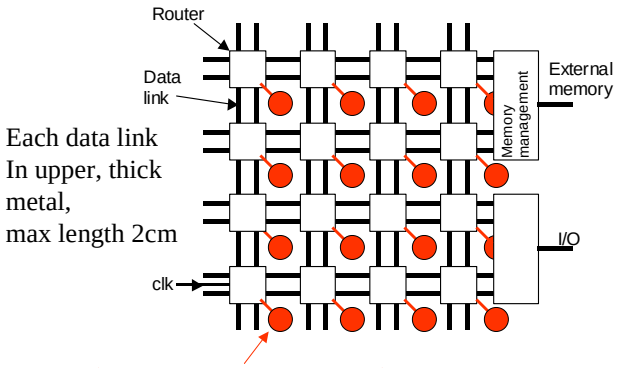
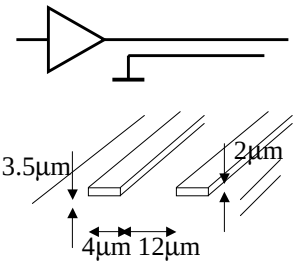
Network-on-Chip example

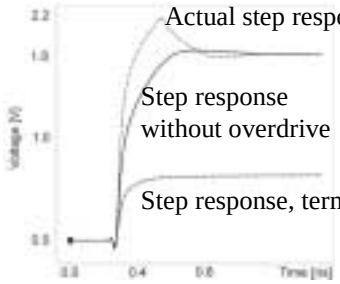


Network-on-Chip example

Wire/driver example

Inverter in 0.18µm CMOS
W_n=88µm, w_p=194µm, R_S=20Ω





Wire length 2cm

2µm x 4µm copper wire, low loss
12µm spacing, X-talk<18%

Network-on-Chip example

Estimated performance

- Simulated velocity: 10^8m/s (c_0/3)
- Simulated maximum data-rate 10Gb/s
- Each link is 16 bit wide, 2 links carry 320Gb/s (bidirectionally)
- Each 2 links need 544µm width

8 by 8 Network:

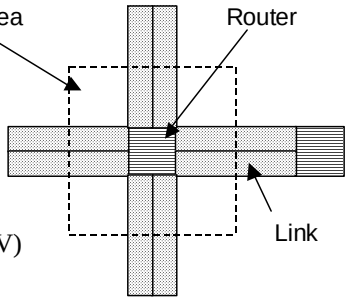
- Bidirectional, bisection bandwidth: 2560Gb/s (also one edge I/O)
- Total bandwidth available to cores: 20480Gb/s
  (if 10% load, still >2Tb/s bandwidth)

Network-on-Chip example

Estimation of space and power

8 by 8 network on 20 by 20 cm chip
31% of one metal layer used

Total power estimated to 1.4W
(at full random data activity and 1.8V)



Conclusions

By utilizing thick upper metal layers (2μm) as microstrip:

- We may reach velocities close to velocity-of-light
- We may reach global (2cm) bandwidths of 10Gb/s

A 8x8 2D Network-on-Chip concept may

- Serve 64 cores with up to 20Tb/s bandwidth
- Sustain 2Tb/s bisection bandwidth
- All at less than 1.4W power consumption