Electrical interconnects revitalized

Christer Svensson
Linköping University

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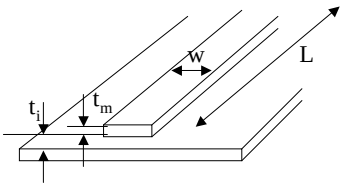
Christer Svensson
Dept. of Electrical Engineering
Linköping University
58183 Linköping, Sweden
Phone: +46 13281223
Fax: +46 13139282
Email: chs@isy.liu.se

Outline

- Introduction
- Modeling transmission lines
- Step response
- Wire performance
- Wires in real systems
- Conclusion

Introduction

Electrical interconnects are considered to be *the* major limitation to performance of scaled electronics.



Wire delay ~ RC

$$RC = \frac{\rho L}{t_m w}\frac{\varepsilon w L}{t_i} = \rho\varepsilon\frac{L^2}{t_m t_i}$$

Wire delay scales as (feature size)$^{-2}$
Logic delay scales as (feature size)

Introduction

Some recent results indicates that this view may be wrong.

The objective of this lecture is to make us understand the *fundamental* limits of electrical interconnects and compare them to optical alternatives.

We want to demonstrate the *opportunities* offered by electrical interconnects.

Introduction

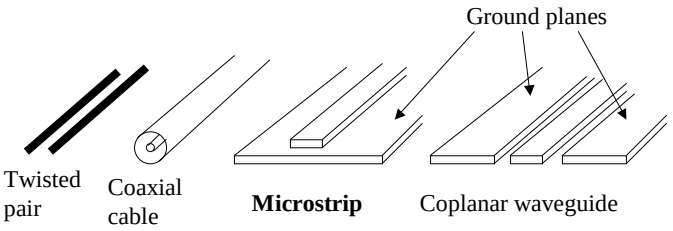
As we are looking for fundamental limits, we will use a *simplified view*: The transmission line view (assuming a well-behaved return path, e.g. a ground plane).

There are two motivations for this simplified view:

• It will give an upper limit to performance, which can be approached in practice.

• It will compare well with alternative solutions, which normally are not implemented and therefore also use simplified views.

Modeling transmission lines



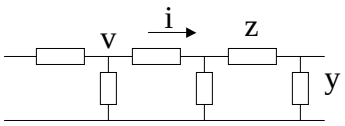
Cables Circuit boards and chips

(Always a return path!)

We will concentrate on microstrip in the following

Modeling transmission lines

Circuit model:



z,y impedance och admittance per unit length

$$\frac{\delta v}{\delta x} = zi \qquad \frac{\delta i}{\delta x} = yv \qquad \Rightarrow \qquad \frac{\delta^2 v}{\delta x^2} = zyv$$

General solution:

$$v = v(0)e^{\pm\sqrt{zy}x} \qquad i = \frac{1}{z}\frac{\partial v}{\partial x} = \pm\sqrt{\frac{y}{z}}v = \frac{v}{Z_c}$$

Modeling transmission lines

Interpretation for a lossless line:

z=jωl, y=jωc $\Rightarrow$ $v = v(0)e^{\pm j\omega\sqrt{lc}x}$

For a sine wave we have: $v = v(0)e^{j\omega(t\pm\sqrt{lc}x)}$ $\quad\quad$ $\upsilon = \dfrac{1}{\sqrt{lc}}$

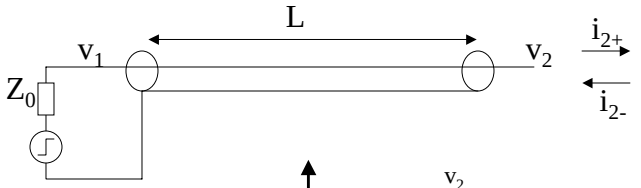
Wave traveling with velocity *v* in positive or negative direction along the line

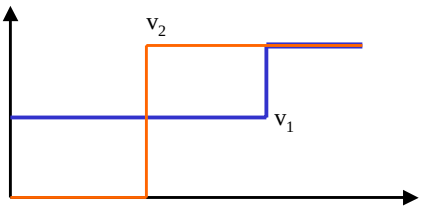
Characteristic impedance: (Real in lossless case) $Z_c = \sqrt{\dfrac{l}{c}} = Z_0$ $\quad$ Typical value 50Ω (20…300Ω)

Also note that $c = 1/\upsilon Z_0$

Modeling transmission lines

Interpretation of signal transfer, an example:





Two waves:
$v_{1,2}=v_+ + v_-$
Open end: $i_2=i_{2+}+i_{2-}=0$
$v_{2-}=-i_{2-}Z_0=i_{2+}Z_0=v_{2+}$
Source end: $v_2/i_2=Z_0$

Modeling transmission lines

Interpretation for a lossy line with simple series resistance:

z=jωl+r, y=jωc $\Rightarrow$ $v = v(0)e^{\pm\sqrt{(j\omega l+r)j\omega c}\,x}$

For small r we have:

$$\sqrt{j\omega c(j\omega l + r)} \approx \sqrt{-\omega^2 lc}\left(1 - j\frac{r}{2\omega l}\right) = j\omega\sqrt{lc} - \frac{r}{2Z_0}$$

Wave attenuated along line

$$v = v(0)e^{-j\omega\sqrt{lc}x}e^{-\frac{r}{2Z_0}x}$$

Characteristic impedance complex

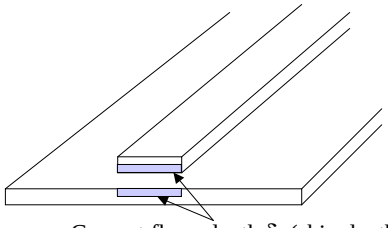
$$Z_c = \sqrt{\frac{j\omega l + r}{j\omega c}}$$

Modeling transmission lines

Skin effect loss

Higher frequencies - skineffekt
Fields penetrate metal to skin-depth δ
Resistance per unit length, r:

$$r = r_s\sqrt{\omega}$$



Current flow, depth δ, (skin depth)

Including current phase and low frequency resistance:

$$r = r_{DC} + r_s(1 + j)\sqrt{\omega}$$

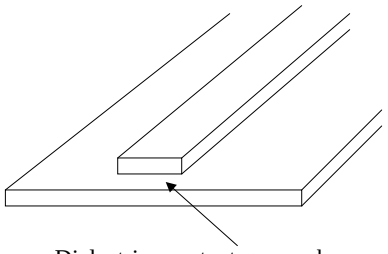
Frequency dependence gives rise to signal distortion

Modeling transmission lines

Dielectric loss

Higher frequencies – dielectric loss
Loss due to molecular movements
(Relaxation loss)

$$\varepsilon = \sum_i \frac{a_i}{1 + j\omega\tau_i}$$



Dielectric constant, ε, may be complex

Frequency dependence gives rise to signal distortion

Most relevant in circuit boards at >10GHz

Modeling transmission lines

Converting to time domain

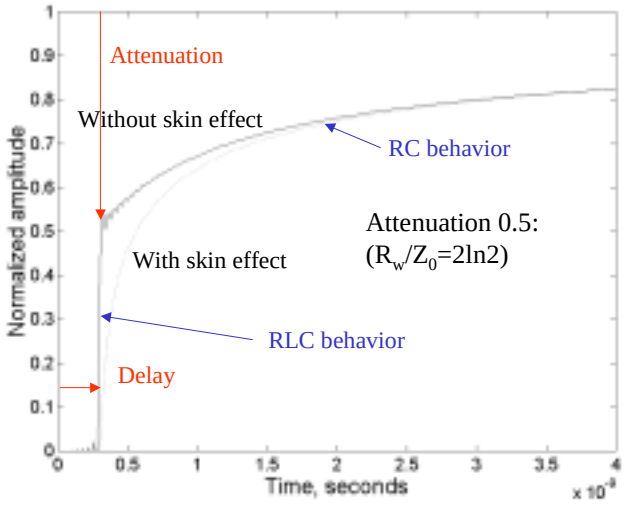
$H = e^{-\sqrt{(j\omega l + r)j\omega c}x}$ Voltage transfer function
Complex and frequency dependent r and c (through ε)

$g = \frac{1}{2}\left(1 + erf\left(a_1\left(t - t_1\right)\right)\right)$ (Step response in time domain)

$v(t) = ifft(HG)$ (Step in time domain)

Step response

Step response of transfer function H



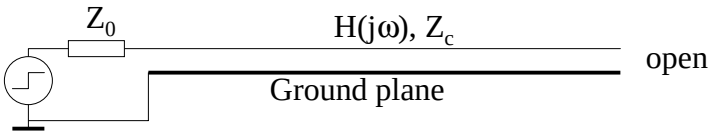
Step response

Large attenuation (R_w/Z_0>>2ln2):
We have a pure RC behaviour
We have very small skin effect

Low attenuation, R_w/Z_0<<2ln2:
We have an RLC behavior (still with loss)
Skin effect dominates resistance

(Note that transfer between RC and RLC resp. DC resistance and skin effect resistance happens to occur at the same point)

Step response of wire with driver



(Solve circuit equations with two waves)

$$v_{out} = \frac{2H}{1+H^2+\frac{Z_0}{Z_c}\left(1-H^2\right)} v_{step}$$

For $Z_c=Z_0$:
$v_{out}=2Hv_{step}$
Step response same as for H

Step response of wire with driver

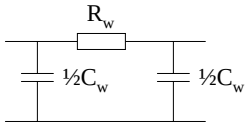
Pure RC case (very large loss)

$$H = e^{-\sqrt{j\omega rc}x} \qquad Z_c = \sqrt{\frac{r}{j\omega c}}$$

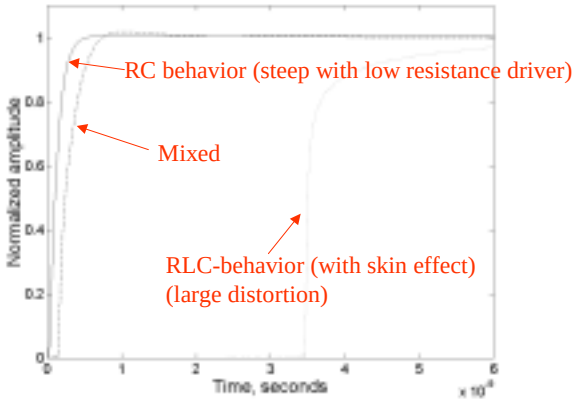
Step response must be calculated from full expression

$$v_{out} = \frac{2Hv_{step}}{1+H^2+\frac{Z_0}{Z_c}\left(1-H^2\right)} \approx \frac{2Hv_{step}}{1+H^2} \approx \frac{v_{step}}{1+\frac{j\omega R_w C_w}{2}}$$

Good approximation:
(lumped model)



Step response of wire with driver



Wire performance

Delay or latency, LC-wire

Delay mainly through velocity, $\mathbf{t_d = vL}$, L=wire length

$$\upsilon = \frac{1}{\sqrt{lc}} = \frac{c_0}{\sqrt{\varepsilon_r}}$$

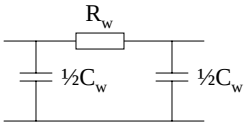
c_0 velocity of light in vacuum, ε_r dielectric constant (square of refractive index)
Note, no higher velocity is possible.

Only difference to optics is the value of refractive index (about 1.9 resp. 1.5)

Wire performance

Delay or latency, RC-wire

RC-wire: Delay mainly through RC charging time, for 50% of final value:



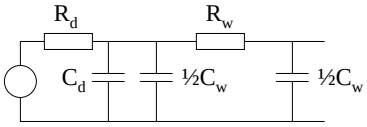
$$t_d = R_w \frac{C_w}{2} \ln 2 = 0.35 \rho \varepsilon \frac{L^2}{t_m t_i}$$

If we assume that a practical wire has a fixed aspect ratio (w/t), we have:

$$t_d = a_{RC} \frac{L^2}{A}$$ A is wire cross section

Wire performance

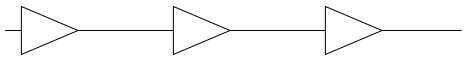
Delay or latency, RC-wire with driver



$t_d = 0.7(R_d(C_d + ½C_w) + (R_d + R_w)½C_w)$

(Elmores delay)

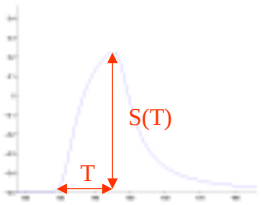
For long wires, delay may be reduced by repeaters:



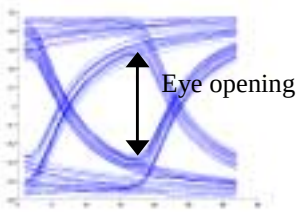
$$t_{d\,\min} \approx \sqrt{t_{invrter} t_{wire}} \propto L$$

Wire performance

Capacity or maximum data rate



Single pulse



Eye diagram

Eye opening = 2S(T)-1, S(t) step response, T symbol time

We need a minimum opening for safe data detection, say 64%

For long wires we may afford a simple equalizer, allowing 0%

Wire performance

Capacity or maximum data rate

RC-wire: Step response: $S(T) = 1 - e^{-\frac{2T}{R_w C_w}}$

Eye opening of 64% yields S(T)=0.82 or $T = 0.85 R_w C_w$

Max data rate $B = \frac{1}{T} = b_{RC} \frac{A}{L^2}$

RLC-wire: Step response (skin effect): $S(T) = 1 - erf\left(\frac{\sqrt{\rho \mu_0} L}{2 Z_0 w \sqrt{T}}\right)$

Max data rate, $B = b_{RLC} \frac{A}{L^2}$

Wire performance

Capacity or maximum data rate

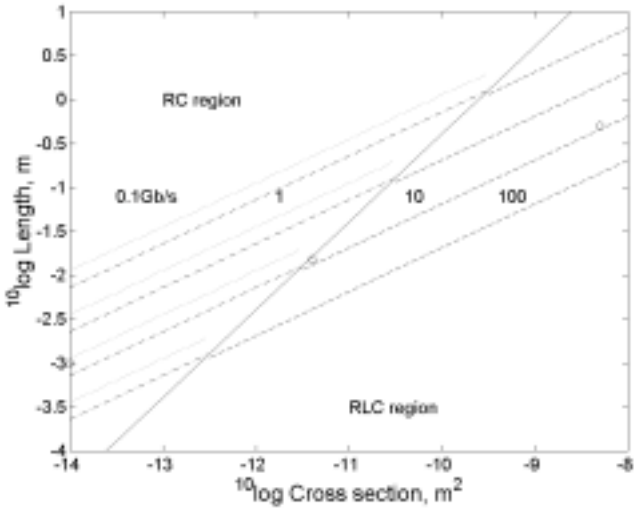
$$B = b\frac{A}{L^2}$$

RC-model (eye opening 64%)	$b_{RC}=5.3\ 10^{17}$ b/s
RC-model (eye opening 0%)	$b_{RC0}=1.3\ 10^{18}$ b/s ($=1/a_{RC}$)
RLC model (eye opening 0%)	$b_{RLC0}=4.3\ 10^{17}$ b/s

For a bus: $A=\Sigma A$

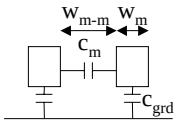
Assumptions: $Z_0=50\Omega$, Copper, Silicon dioxide

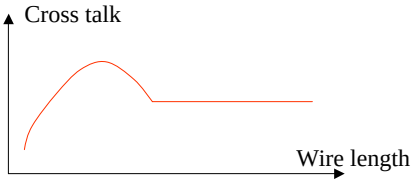
Estimated data rates



Wire performance

Crosstalk





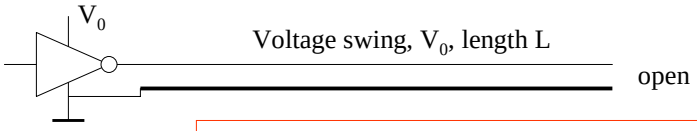
$$\text{Peak crosstalk} \approx \frac{\pi}{4}\frac{c_m}{c_{grd}+c_m}$$

Realistic wires (aspect ratio 3) need w_{m-m} ~1.5w_m to limit crosstalk to 20%

(J. A. Davis and J. D. Meindl, IEEE Trans. Electronic Devices, vol. 47, p. 2078, 2000)

Wire performance

Power consumption



Inverter with output resistance Z_0

Random data

$T_D = L/v$

Data rate: f=1/T

Current consumption:

$$\bar{I} = \frac{1}{4} fCV_0 \quad \text{For } 2T_D < T$$

$$\bar{I} = \frac{V_0}{8Z_0} \quad \text{For } 2T_D > T$$

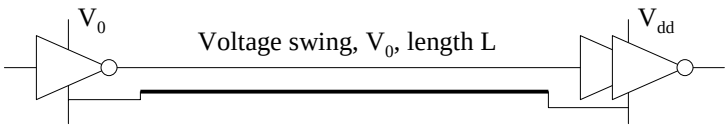
Power Consumption:

$$P_{wire} = \bar{I}V_0 \quad V_0 \text{ is supply}$$

$$P_{wire} = \bar{I}V_{dd} \quad \text{Separate supply}$$

Wire performance

Power optimum voltage swing



Using reduced swing to save power needs an amplifier for restoring swing to V_{dd}

$$P = P_{wire} + P_{ampl}$$

The total power shows a minimum for a particular swing, V_{0opt}

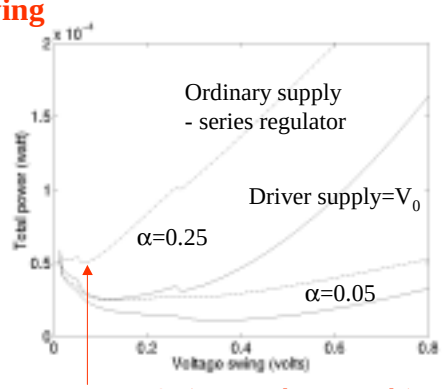
Wire performance

Power optimum voltage swing (Example)

Process: (Inverters as amplifiers)
V_{dd}=1.3V, V_T=0.3V, G_{max}=5

General:
C_L=10fF, C_w=1pF, f_c=1GHz,
α=0.05 and 0.25

α=activity (f/f_c)



Optimum swing ~ 60 mV @ α=0.25; power saving 8x (Using ordinary supply); two stage amplifier

Wires in real systems

We will examine three cases and draw some practical conclusions from these

Wires on circuit boards

Global wires on chip

Local wires on chip

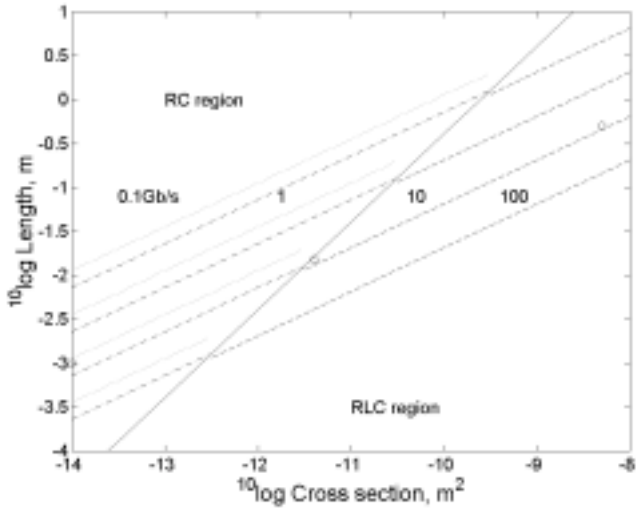
Wires in real systems

Wire on circuit board:
Far into RLC region: $A=5\cdot10^{-9}$ m^2, L=0.5m B=10Gb/s
Delay=3.3ns (velocity of light in polymer)

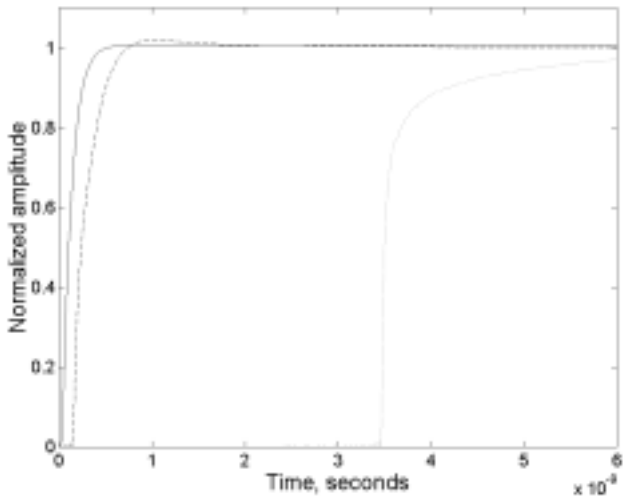
Upper level chip wire:
At borderline: $A=4\cdot10^{-12}$ m^2, L=1.5cm B=20Gb/s
Delay≈100ps (RLC-model)

Lower level chip wire
Far into RC region: $A=10^{-14}$ m^2, L=1mm, B=5Gb/s
Delay=80ps

Wires in real systems



Wires in real systems

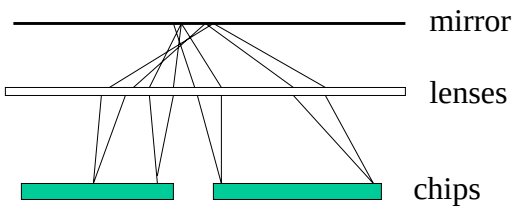


Chip I/O capacity

Typical board wire: 0.25mmx20µm=5 $10^{-9}m^2$
10Gb/s 0.5m, more than a full board!

Chip edge capacity: Bus effective cross section: 2cmx20µm/2.5
(assuming chip edge 2cm and wire to wire distance 1.5x(wire width)
length 10cm
gives bus capacity B=6.8Tb/s
Can be implemented with 340 wires at 20Gb/s each.
Pitch 58µm, quite possible
Total chip I/O: 27.2Tb/s (using 4 edges)

Optical example



Example from literature: 4Tb/s for $4cm^2$ area
Total power 4W (my optimistic view)
(Electrical case estimated optimal power 0.1W at 120mV swing)
(Kibar, VanBlerkom, Fan, Esener, J Lightwave Techn., vol. 17, p. 546, 1999)

On-chip global

Keeping full light velocity needs $R_w < Z_0 2\ln 2$
For 2cm chip, max length (Manhattan) 4cm
Then we need $A=10^{-11}m^2$
Not unrealistic; example $3.2x3.2\mu m^2$
(Microprocessor of today, 2.2µm thick outer metal)
B=8Gb/s

Bus capacity across chip: A=2cmx3µm/2.5 L=2cm
B=77Tb/s (compare external edge: 6.8Tb/s)
(2700 wires of 3µm at 28Gb/s; total power 2.7W
@ 90mV swing)

On-chip local

Future processes, feature size f=0.1 - 0.035 µm
wire cross section ~$3f^2$, for 0.1µm: $3 \cdot 10^{-14}m^2$
10Gb/s up to 1.25mm length
1mm wire will have a delay of 26ps (26% of 10GHz clock cycle)

We may use 10GHz clock frequency in fully synchronous block of diameter 1mm. Such a block can contain 250,000 gates.
(Compare to Sylvester and Keutzler 50-100 kgates)

Note that diameter scales as f^2; number of gates as f^{-2}
so 250 kgates is kept until 0.035µm (or further) at 10GHz.

Clock distribution

For clock distribution the only critical issue is to distribute a constant frequency with equal delay to each target

Using a balanced H-tree allows equal delay
H-tree over 2x2cm^2 chip, longest path <2cm

A=10^{-11} m^2 (as above), L=2cm, total delay ~130ps

A=10^{-11} m^2, L=2cm: 50% attenuation at 22GHz (T=45ps)

Conclusions

Electrical interconnects are still very effective

We may have a total I/O capacity of 25Tb/s.
(Optical can not compete at short distances (on board))

An upper metal may carry 70Tb/s across chip, with a delay corresponding to light velocity

Full synchronism can be used at 10GHz clock in blocks containing >200kgates (diameter 1mm in 0.1µm process)

On-chip global clock distribution up to 20GHz possible

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